

09/719440

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Practitioner's Docket No. 870-003-128

CHAPTER II

Preliminary Classification:

Proposed Class:

Subclass:

NOTE: "All applicants are requested to include a preliminary classification on newly filed patent applications. The preliminary classification, preferably class and subclass designations, should be identified in the upper right-hand corner of the letter of transmittal accompanying the application papers, for example 'Proposed Class 2, subclass 129.' " M.P.E.P., § 601, 7th ed.

**TRANSMITTAL LETTER
TO THE UNITED STATES ELECTED OFFICE (EO/US)**

(ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP99/03992	10.06.99	13.06.98

TITLE OF INVENTION

Device with an Electromotor

APPLICANT(S)

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KALTENBRUNNER

Box PCT

Assistant Commissioner for Patents

Washington D.C. 20231

ATTENTION: EO/US

CERTIFICATION UNDER 37 C.F.R. § 1.10*

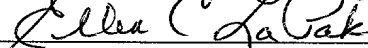
(Express Mail label number is mandatory.)

(Express Mail certification is optional.)

I hereby certify that this Transmittal Letter and the papers indicated as being transmitted therewith is being deposited with the United States Postal Service on this date Dec. 12, 2000, in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EL 628 639 832 IIS, addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231.

~~Judith Schrick~~ Ellen C. LaPak

(type or print name of person mailing paper)



Signature of person mailing paper

WARNING: Certificate of mailing (first class) or facsimile transmission procedures of 37 C.F.R. § 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.

***WARNING:** Each paper or fee filed by "Express Mail" **must** have the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 C.F.R. § 1.10(b).

"Since the filing of correspondence under § 1.10 without the Express Mail mailing label thereon is an oversight that can be avoided by the exercise of reasonable care, requests for waiver of this requirement will **not** be granted on petition." Notice of Oct. 24, 1996, 60 Fed. Reg. 56,439, at 56,442.

(Transmittal Letter to the United States Elected Office (EO/US) [13-18]—page 1 of 8)

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2. Fees

CLAIMS FEE	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
<input type="checkbox"/> *	TOTAL CLAIMS	37 - 20 =	17	× \$18.00 =	\$ 306.
	INDEPENDENT CLAIMS	4 - 3 =	1	× \$78.00 =	80.
	MULTIPLE DEPENDENT CLAIM(S) (if applicable) + \$260.00				
BASIC FEE**	<input type="checkbox"/> U.S. PTO WAS INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where an international preliminary examination fee as set forth in § 1.482 has been paid on the international application to the U.S. PTO: <ul style="list-style-type: none"> <input type="checkbox"/> and the international preliminary examination report states that the criteria of novelty, inventive step (non-obviousness) and industrial activity, as defined in PCT Article 33(1) to (4) have been satisfied for all the claims presented in the application entering the national stage (37 C.F.R. § 1.492(a)(4)) \$96.00 <input type="checkbox"/> and the above requirements are not met (37 C.F.R. § 1.492(a)(1)) \$670.00 <input type="checkbox"/> U.S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in § 1.482 has been paid to the U.S. PTO, and payment of an international search fee as set forth in § 1.445(a)(2) to the U.S. PTO: <ul style="list-style-type: none"> <input type="checkbox"/> has been paid (37 C.F.R. § 1.492(a)(2)) \$690.00 <input type="checkbox"/> has not been paid (37 C.F.R. § 1.492(a)(3)) \$970.00 <input checked="" type="checkbox"/> where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 C.F.R. § 1.492(a)(5)) \$840.00 860. 				
	Total of above Calculations				= 1246.
SMALL ENTITY	Reduction by 1/2 for filing by small entity, if applicable. Affidavit must be filed also. (note 37 C.F.R. § 1.9, 1.27, 1.28)				-
	Subtotal				
	Total National Fee				\$ 1246.
	Fee for recording the enclosed assignment document \$40.00 (37 C.F.R. § 1.21(h)). (See Item 13 below). See attached "ASSIGNMENT COVER SHEET".				40.
TOTAL	Total Fees enclosed				\$ 1286.

*See attached Preliminary Amendment Reducing the Number of Claims.

- i. ☒ A check in the amount of 1286 to cover the above fees is enclosed.
- ii. ☒ Please charge Account No. 23-0442 in the amount of \$.
A duplicate copy of this sheet is enclosed. *For any deficiency*

****WARNING:** "To avoid abandonment of the application the applicant shall furnish to the United States Patent and Trademark Office not later than the expiration of 30 months from the priority date: * * * (2) the basic national fee (see § 1.492(a)). The 30-month time limit may not be extended." 37 C.F.R. § 1.495(b).

WARNING: If the translation of the international application and/or the oath or declaration have not been submitted by the applicant within thirty (30) months from the priority date, such requirements may be met within a time period set by the Office. 37 C.F.R. § 1.495(b)(2). The payment of the surcharge set forth in § 1.492(e) is required as a condition for accepting the oath or declaration later than thirty (30) months after the priority date. The payment of the processing fee set forth in § 1.492(f) is required for acceptance of an English translation later than thirty (30) months after the priority date. Failure to comply with these requirements will result in abandonment of the application. The provisions of § 1.136 apply to the period which is set. Notice of Jan. 3, 1993, 1147 O.G. 29 to 40.

3. ☒ A copy of the International application as filed (35 U.S.C. § 371(c)(2)):

NOTE: Section 1.495 (b) was amended to require that the basic national fee and a copy of the international application must be filed with the Office by 30 months from the priority date to avoid abandonment. "The International Bureau normally provides the copy of the international application to the Office in accordance with PCT Article 20. At the same time, the International Bureau notifies applicant of the communication to the Office. In accordance with PCT Rule 47.1, that notice shall be accepted by all designated offices as conclusive evidence that the communication has duly taken place. Thus, if the applicant desires to enter the national stage, the applicant normally need only check to be sure the notice from the International Bureau has been received and then pay the basic national fee by 30 months from the priority date." Notice of Jan. 7, 1993, 1147 O.G. 29 to 40, at 35-36. See item 14c below.

- a. ☒ is transmitted herewith.
- b. ☐ is not required, as the application was filed with the United States Receiving Office.
- c. ☐ has been transmitted
 - i. ☐ by the International Bureau.
Date of mailing of the application (from form PCT/1B/308): .
 - ii. ☐ by applicant on .
Date

4. ☒ A translation of the International application into the English language (35 U.S.C. § 371(c)(2)):

- a. ☒ is transmitted herewith.
- b. ☐ is not required as the application was filed in English.
- c. ☐ was previously transmitted by applicant on .
Date
- d. ☐ will follow.

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5. ☒ Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. § 371(c)(3)):

NOTE: The Notice of January 7, 1993 points out that 37 C.F.R. § 1.495(a) was amended to clarify the existing and continuing practice that PCT Article 19 amendments must be submitted by 30 months from the priority date and this deadline may not be extended. The Notice further advises that: "The failure to do so will not result in loss of the subject matter of the PCT Article 19 amendments. Applicant may submit that subject matter in a preliminary amendment filed under section 1.121. In many cases, filing an amendment under section 1.121 is preferable since grammatical or idiomatic errors may be corrected." 1147 O.G. 29-40, at 36.

- a. ☒ are transmitted herewith.
- b. ☐ have been transmitted
- i. ☐ by the International Bureau.
Date of mailing of the amendment (from form PCT/1B/308): _____
- ii. ☐ by applicant on (date) _____
Date
- c. ☐ have not been transmitted as
- i. ☐ applicant chose not to make amendments under PCT Article 19.
Date of mailing of Search Report (from form PCT/ISA/210.): _____
- ii. ☐ the time limit for the submission of amendments has not yet expired.
The amendments or a statement that amendments have not been made will be transmitted before the expiration of the time limit under PCT Rule 46.1.

6. ☒ A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. § 371(c)(3)):
- a. ☒ is transmitted herewith.
- b. ☐ is not required as the amendments were made in the English language.
- c. ☐ has not been transmitted for reasons indicated at point 5(c) above.

7. ☒ A copy of the international examination report (PCT/IPEA/409)
- ☒ is transmitted herewith.
- ☐ is not required as the application was filed with the United States Receiving Office.

8. ☐ Annex(es) to the international preliminary examination report
- a. ☐ is/are transmitted herewith.
- b. ☐ is/are not required as the application was filed with the United States Receiving Office.

9. ☐ A translation of the annexes to the international preliminary examination report
- a. ☐ is transmitted herewith.
- b. ☐ is not required as the annexes are in the English language.

10. ☒ An oath or declaration of the inventor (35 U.S.C. § 371(c)(4)) complying with 35 U.S.C. § 115
- a. ☐ was previously submitted by applicant on _____
Date
- b. ☒ is submitted herewith, and such oath or declaration
- i. is attached to the application.
- ii. ☒ identifies the application and any amendments under PCT Article 19 that were transmitted as stated in points 3(b) or 3(c) and 5(b); and states that they were reviewed by the inventor as required by 37 C.F.R. § 1.70.
- c. ☐ will follow.

II. Other document(s) or information included:

11. ☒ An International Search Report (PCT/ISA/210) or Declaration under PCT Article 17(2)(a):
- a. ☒ is transmitted herewith. *as mailed 23 Nov. 1999*
- b. ☐ has been transmitted by the International Bureau.
Date of mailing (from form PCT/IB/308): _____
- c. ☐ is not required, as the application was searched by the United States International Searching Authority.
- d. ☐ will be transmitted promptly upon request.
- e. ☐ has been submitted by applicant on _____
Date
12. ☒ An Information Disclosure Statement under 37 C.F.R. §§ 1.97 and 1.98:
- a. ☒ is transmitted herewith.
Also transmitted herewith is/are:
- ☒ Form PTO-1449 (PTO/SB/08A and 08B).
- ☒ Copies of citations listed.
- b. ☐ will be transmitted within THREE MONTHS of the date of submission of requirements under 35 U.S.C. § 371(c).
- c. ☐ was previously submitted by applicant on _____
Date
13. ☒ An assignment document is transmitted herewith for recording.
A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☒ FORM PTO 1595 is also attached.
- _____
- _____
- _____

14. ☒ Additional documents:

- a. ☐ Copy of request (PCT/RO/101)
- b. ☒ International Publication No. WO 99/6633
 - i. ☒ Specification, claims and drawing
 - ii. ☐ Front page only
- c. ☒ Preliminary amendment (37 C.F.R. § 1.121)
- d. ☐ Other

15. ☒ The above checked items are being transmitted

- a. ☒ before 30 months from any claimed priority date.
- b. ☐ after 30 months.

16. ☐ Certain requirements under 35 U.S.C. § 371 were previously submitted by the applicant on _____, namely:

AUTHORIZATION TO CHARGE ADDITIONAL FEES

WARNING: Accurately count claims, especially multiple dependant claims, to avoid unexpected high charges if extra claims are authorized.

NOTE: "A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).

NOTE: "Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).

☒ The Commissioner is hereby authorized to charge the following additional fees that may be required by this paper and during the entire pendency of this application to Account No. 23-0442.

☒ 37 C.F.R. § 1.492(a)(1), (2), (3), and (4) (filing fees)

WARNING: Because failure to pay the national fee within 30 months without extension (37 C.F.R. § 1.495(b)(2)) results in abandonment of the application, it would be best to always check the above box.

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☒ 37 C.F.R. § 1.492(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1.492(d)), it might be best not to authorize the PTO to charge additional claim fees, except possible when dealing with amendments after final action.

☐ 37 C.F.R. § 1.17 (application processing fees)☐ 37 C.F.R. § 1.17(a)(1)–(5) (extension fees pursuant to § 1.136(a).☐ 37 C.F.R. § 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. § 1.311(b))

NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 C.F.R. § 1.311(b).

NOTE: 37 C.F.R. § 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying . . . issue fee." From the wording of 37 C.F.R. § 1.28(b): (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

☒ 37 C.F.R. § 1.492(e) and (f) (surcharge fees for filing the declaration and/or filing an English translation of an International Application later than 30 months after the priority date).


SIGNATURE OF PRACTITIONER

Milton Oliver

(type or print name of practitioner)

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IN THE U.S. PATENT & TRADEMARK OFFICE

Applicants: KARWATH et al.
Serial #: 09/_____ = § 371 of PCT/EP99/03992
Filed: DEC. 12, 2000 (HEREWITH)
Title: DEVICE WITH AN ELECTROMOTOR
Art Unit: 2107 Examiner: Not yet assigned

PRELIMINARY AMENDMENT TO PCT APPLICATION

Assistant Commissioner for Patents DEC. 12, 2000
Washington, D.C. 20231

Sir:

Prior to counting the claims,
please amend the application as follows:

IN THE SPECIFICATION:

Please cancel original page 1 and substitute therefor the
attached new pages 1 and 1A.

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PCT/EP99/03992

DEVICE WITH AN ELECTROMOTOR

FIELD OF THE INVENTION:

The invention concerns an arrangement having an electric motor, and in particular having an electronically commutated motor (ECM).

BACKGROUND: Examples of such motors are shown, for example, in the following documents [of the Applicant] assigned to the assignee of the present application:

DE 44 41 372 A1	[(internal: D183)]	= 5,845,045 JESKE
EP 0 658 973 B1	[(internal: EP184)]	= 5,590,235 JESKE
DE 296 06 939.6-U	[(internal: D190i)]	= EP 0 739 084 A2
DE 195 15 944 A1	[(internal: D192)]	
EP 0 741 449 A1	[(internal: EP193)]	= 6,163,117
EP 0 744 807 B1	[(internal: EP194)]	= 5,847,523
DE 195 18 991 A1	[(internal: D195)]	
DE 196 47 983 A1	[(internal: D199i)]	= 6,091,887
EP 0 780 962 A2	[(internal: EP200)]	

It would not be possible to reproduce the extensive content of these documents even in summarized form, and reference is therefore made to their complete contents.

SUMMARY OF THE INVENTION:

It is an object of the invention to make available a new arrangement and a new method for controlling an electric motor.

According to the invention, this object is achieved by connecting an output signal of a microprocessor, which can take on either a high level or a low level, to a voltage divider which regulates motor current, and varying the microprocessor output signal to achieve a desired motor current characteristic curve.

[the subject matter of claim 1]. It is possible thereby, in program-controlled fashion, either to extend acceleration (called a "soft start") or to make acceleration as short as possible by

raising the operating point for the current control system during the acceleration period so that the motor current can be higher during acceleration than later in normal operation.

A preferred method is to set a motor current limit to a first value for motor startup, to monitor the startup, and to reset the motor current limit to a second value after startup. [the subject matter of claim 11]. This method can be flexibly adapted to the needs of a user, since the limiting values can be adjusted in program-controlled fashion.

Page 2, lines 20-21, insert a period after "invention)" and
cancel ", and from the other dependent claims. In the drawings:"

Page 2, after line 21, insert: --BRIEF FIGURE DESCRIPTION:--.

Page 4, after line 3, insert --DETAILED DESCRIPTION:--.

Page 32, line 1, change "Claims"

to --WHAT IS CLAIMED IS:--.

Page 38, change "Abstract"

to --ABSTRACT OF THE DISCLOSURE--.

IN THE CLAIMS:

1. (Amended) An arrangement [having] comprising
an electric motor (10; 10'), [having a microcontroller (12)
or microprocessor, hereinafter simply called] and
a microprocessor (12), for influencing at least one motor
function, having a terminal (A), wherein [which arrangement]
an output on said terminal (A) of the microprocessor (12) [can be
switched over] is switchable in program-controlled fashion [to]
between a high level [or to] and a low level; and
further comprising a first voltage divider (20, 22) having
a tapping point (18) thereof [(19) of a first voltage divider
(20, 22) is] connected to [that] said terminal (A) via a resistor
(17) in order to make the potential of that voltage divider
tapping point (18) switchable in program-controlled fashion
between at least two values by modifying that level, and by
[way of that] switching said potential, to influence a parameter
of the motor (10; 10').

2. (Amended) The arrangement as defined in claim 1, wherein
[which]
the parameter is a current limiting value (I_{ref}) for
limiting [the] motor current (i) of the electric motor (10; 10').

3. (Amended) The arrangement as defined in claim 1 [or 2],
wherein [which] said resistor (17) is of high-resistance
configuration.

4. (Amended) The arrangement as defined in claim 3,
wherein [which] the value of said resistor (17) is not less than
50 kilohm [or more].

5. (Amended) The arrangement as defined in [one or more of] claim[s] 1 [through 4], wherein [which] said output [(A)] of the microprocessor (12) [can be switched over] is switchable in program-controlled fashion to a third, high-resistance, state [(FIG. 4)].

6. (Amended) The arrangement as defined in [one or more of the foregoing claims] claim 1, wherein said first voltage divider has branches and [which]

there is provided, parallel to one branch (22) of the first voltage divider (20, 22), a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) influencing the parameter of the motor (10; 10').

7. (Amended) The arrangement as defined in claim 6, wherein [which] the second voltage divider (160) has a higher resistance as compared to the resistance value of the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

8. (Amended) The arrangement as defined in claim 6 [or 7], wherein [which] the voltage division ratio of the second voltage divider (60) is designed so that, when the potential at its tapping point (163) is used as a comparison potential, the result is a low[er] value for that comparison potential.

9.(Amended) The arrangement as defined in [one of more of] claim[s] 6 [through 8, in which] wherein

the potential at the tapping point (163) of the second voltage divider (160) defines a current limiting value (I_{ref}) for limiting the motor current (i) of the electric motor (10; 10').

10.(Amended) The arrangement as defined in claim 2 [or 9], [having] comprising

a nonvolatile memory element (14) [which serves] serving to store at least one time value (T_s) after whose expiration a switchover of said output (A) of the microprocessor (12) is accomplished in program-controlled fashion.

Please add a new dependent claim:

41. The arrangement as defined in claim 9, comprising a nonvolatile memory element (14) serving to store at least one time value (T_s) after whose expiration a switchover of said output (A) of the microprocessor (12) is accomplished in program-controlled fashion.

11.(Amended) A method [for] of controlling the startup of an electric motor [with which a microcontroller or microprocessor, hereinafter called] comprising

an associated control circuit including a microprocessor (12), a nonvolatile memory [element] (14), a data bus (13, 15) interconnecting said microprocessor and memory element, and an arrangement, coupled to an output of said microprocessor, for limiting the motor current (i), [are associated for control purposes, the method having] comprising the following steps:

storing, in the nonvolatile memory, [an acceleration] a startup time (Ts) [is stored] via the data bus (13, 15) [in the nonvolatile memory element (14)];

switching on [after] the motor [is switched on, that] and thereafter monitoring the startup time (Ts) of said motor [acceleration time (TS) is monitored];

during [that acceleration] said startup time (Ts), setting, under control of a program running in said microprocessor, a [the] current limiting value (Iref), of the arrangement for limiting the motor current (i), [is set in program-controlled fashion] to a first value (Iref = 1);

[when it is ascertained that the] ascertaining expiration of said startup [acceleration] time (Ts) [has expired,] and thereafter, in a program-controlled manner, setting the current limiting value (Iref) [is switched over in program-controlled fashion] to a second value (Iref = TST) that is different from the first value.

12. (Amended) The method as defined in claim 11, wherein [which] the second current limiting value is less than the first current limiting value.

13. (Amended) The method as defined in claim 11 [or 12], further comprising [in which, after]

upon expiration of the acceleration time (Ts) [has expired], [a determination is made as to] determining whether motor current limiting [is] has been effective during a time span that exceeds a predefined time span;

and if such [is the case] current limiting has been effective during said time span, changing the current limiting value (Iref) [is switched over] in program-controlled fashion to a third value (Iref = 0).

14. (Amended) An arrangement for carrying out [the method as defined in one or more of claims 11 through 13,] program-controlled adjustment of limitation of current passing through windings of a motor controlled by an associated microprocessor (12) wherein [which]

the microprocessor (12), for program-controlled switchover of [the] a current limiting value (Iref), comprises [has] at least one terminal whose output signal [(A) that can be switched over] is switchable at least between a high and a low signal level and thereby influences the current limiting value (Iref);

and [that] wherein said output signal level is modifiable [can be modified] in program-controlled fashion during [acceleration] startup of the motor (10; 10').

15. (Amended) The arrangement as defined in claim 14, wherein [which] the at least one output (A) [can be switched over] is switchable to a high-resistance state called the tristate state.

16. (Amended) The arrangement as defined in claim 14 [or 15], wherein [which] the output (A) serving to switch over the current limiting value is connected via a resistor (17) to [the] a tapping point (18) of a first voltage divider (20, 22), the potential at that tapping point (18) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows;

and wherein the motor current (i) [being] is interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

17. (Amended) The arrangement as defined in claim 16, wherein [which] there is provided, parallel to one branch (22) of the first voltage divider (20, 22), a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows;

and wherein the motor current (i) [being] is interrupted when that voltage (u) reaches a predefined ratio with respect to that potential at the latter tapping point (163).

18.(Amended) The arrangement as defined in claim 17, [in which] further comprising a comparator (28) is [provided for] serving to make a comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows.

19.(Amended) The arrangement as defined in claim 17 [or 18], wherein [which] the second voltage divider (160) has a higher resistance as compared to the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

20.(Amended) The arrangement as defined in [one or more of] claim[s] 17 [through 19], wherein [which the] a voltage division ratio of the second voltage divider (60) is [designed] so chosen that, when the potential at its tapping point (163) is used as a comparison potential, the result is a low[er] value for that comparison potential.

21.(Amended) The arrangement as defined in [one or more of] claim[s] 18 [16 through 20], wherein [which] the voltage (u) at the measurement resistor (36) is filtered [through] by a low-pass [element] filter (38, 42) before comparison with the aforesaid comparison potential.

22.(Amended) The arrangement as defined in claim 21, [in which] wherein the low-pass element is configured as a first-order low-pass [element] filter (38, 42).

23. (Amended) An arrangement [having] comprising
an electric motor (10; 10'), [in particular] adapted for
driving a fan (73), [having a microcontroller (12) or
microprocessor, hereinafter simply called]

a microprocessor (12), for influencing at least one motor
function, there being associated with that microprocessor (12)
a volatile memory element (330) and a nonvolatile memory element
(14), [which] said memory elements being configured for storing
at least one object as a definition for that motor function;

[further having] an interface (13a), associated with the
electric motor, for a data line (13; 210, 226) for transferring
that at least one object [to and/or from] between said
microprocessor and a memory element (14, 330),

and [having]

a stored directory (280), associated with the microprocessor
(12), which contains, for objects that are transferable via the
data line (13, 210, 226), predefined parameters (286, 288, 290)
for the transfer of those objects.

24. (Amended) The arrangement as defined in claim 23, [in
which] wherein

the stored directory (280) contains data (286)
as to the length of transferable objects.

25. (Amended) The arrangement as defined in claim 23 [or
24, in which] wherein

the stored directory (280) contains data (288) as to whether
the relevant object is intended for storage in the nonvolatile
memory element (14) or in a volatile memory element (330).

26.(Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 25], wherein [which]
the stored directory (280) contains data (290)
as to the address of the object in a memory element (14, 330).

27.(Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 26, in which] wherein
the stored directory (280) is stored in a nonvolatile and
[, in particular,] permanent fashion in a memory (336) associated
with the microprocessor (12).

28.(Amended) The arrangement as defined in claim 27,
wherein [which]
the stored directory (280) is a hardware component of the
microprocessor (12).

29.(Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 28], wherein [which]
the microprocessor (12) is connected to the interface (13a)
for the data line (13);
and the transfer of objects from and/or to the nonvolatile
memory element (14) is accomplished via the microprocessor (12).

30.(Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 29], wherein [which] the data line
is [configured as] a serial data bus (13, 210, 226).

31.(Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 30, in which] wherein at least one buffer memory (332) for data traffic with a data line (13; 15) is provided in the volatile memory (330) associated with the microprocessor (12).

32.(Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 31, in which] wherein the nonvolatile memory element (14) is connected [via a line (CS)] to the microprocessor (12) via a line (CS) which, controlled by the microprocessor (12), influences a write protection of the nonvolatile memory element (14).

33.(Amended) The arrangement [as defined in one or more of] according to claim[s] 23 [through 32, in which] wherein the microprocessor (12) comprises [has]

a predefined memory element (332) for storing an address [(FIG. 17: 242; FIG. 18: 254)] conveyed via the data line (13), an arrangement (14, 330) for storing an address (324) of the arrangement to be addressed, and a comparator[ison arrangement] for comparing those two addresses.

34. (Amended) The arrangement [as defined in one or more of] according to claim[s] 23 [through 33, in which] wherein a memory element (332) is for storing a variable [(FIGS. 18, 19: 246; FIG. 18: 254)] that characterizes an object to be transferred, is associated with the microprocessor (12); and by [way of] using that variable, at least one characteristic (286, 288, 290) of that object can be [taken] retrieved, for processing thereof, from a directory (280) stored in the arrangement.

35. (Amended) The arrangement as defined in claim 34, wherein [which] the characteristic is the length (286) of that object.

36. (Amended) The arrangement as defined in claim 34 [or 35, in which] wherein the characteristic is the hardware address (288, 290) of that object.

Please cancel claims 37-40, without prejudice.

REMARKS

Applicants have made the foregoing amendments to place the PCT application text in customary US format, so that all the claims can be considered on their merits. All multiple dependencies have been cancelled. Claims 37-38 have been cancelled, and a new claim 39 has been added. Most of the foreign documents (or their English equivalents) mentioned in the specification are included in the Information Disclosure Statement filed herewith. New specification pages 1 & 1A, which identify the corresponding US cases owned by Papst and which paraphrase claims 1 and 11 instead of referring to their content, are enclosed herewith.

If the Patent Office notes any remaining informalities which would prevent or hinder examination on the merits, a telephone call to Applicants' counsel is requested.

Respectfully submitted,

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DEVICE WITH AN ELECTROMOTOR

1 The invention concerns an arrangement having an
2 electric motor, and in particular having an electronically
3 commutated motor (ECM).

4 Examples of such motors are shown, for example, in the
5 following documents of the Applicant:

6 DE 44 41 372 A1 (internal: D183)
7 EP 0 658 973 B1 (internal: EP184)
8 DE 296 06 939.6-U (internal: D190i)
9 DE 195 15 944 A1 (internal: D192)
10 EP 0 741 449 A1 (internal: EP193)
11 EP 0 744 807 B1 (internal: EP194)
12 DE 195 18 991 A1 (internal: D195)
13 DE 196 47 983 A1 (internal: D199i)
14 EP 0 780 962 A2 (internal: EP200)

15 It would not be possible to reproduce the extensive
16 content of these documents even in summarized form, and
17 reference is therefore made to their complete contents.

18 It is an object of the invention to make available a
19 new arrangement and a new method for controlling an electric
20 motor.

21 According to the invention, this object is achieved by
22 the subject matter of claim 1. It is possible thereby, in
23 program-controlled fashion, either to extend acceleration
24 (called a "soft start") or to make acceleration as short as
25 possible by raising the operating point for the current
26 control system during the acceleration period so that the
27 motor current can be higher during acceleration than later
28 in normal operation.

29 A preferred method is the subject matter of claim 11.
30 This method can be very flexibly adapted to the needs of a
31 user, since the limiting values can be adjusted in program-
32 controlled fashion.

1 Another manner of achieving the stated object is the
2 subject matter of claim 23. In this fashion, it is easily
3 possible to adapt this kind of arrangement having an
4 electric motor to the needs of its user by entering the
5 desired values via the interface into the nonvolatile memory
6 element of the arrangement (or reading it out from said
7 memory element). This applies in principle to all motor
8 values, e.g. rotation speed, current limiting values,
9 temperature, acceleration time, torque at rest, and others.
10 The storage operation can be accomplished at the factory or
11 at a later point in time in order to adapt the motor
12 optimally to a customer's needs. This is particularly
13 advantageous for motors that drive a fan, since with such
14 fans the needs of users can be very different, and a fan
15 arrangement of this kind can very easily be optimized for a
16 user's needs, as depicted for example in FIG. 22.

17 Further details and advantageous developments of the
18 invention are evident from the exemplary embodiments
19 described below and depicted in the drawings (and to be
20 understood in no way as a limitation of the invention), and
21 from the other dependent claims. In the drawings:

22 FIG. 1 is a schematic circuit diagram of an arrangement
23 according to the present invention;

24 FIGS. 2-4 are circuit diagrams to explain FIG. 1;

25 FIG. 5 is a flow chart to explain the mode of operation
26 of the arrangement according to FIGS. 1 through 4;

27 FIG. 6 shows an exemplary embodiment of a motor
28 arrangement that can be used in the arrangement shown in
29 FIG. 1;

30 FIG. 7 is a view to explain FIG. 5;

31 FIG. 8 is a further depiction to explain the invention;

32 FIG. 9 shows an exemplary depiction of the invention in
33 combination with an electronically commutated motor 10';

34 FIG. 10 shows the terminal markings of the COP 842 CJ
35 microcontroller;

1 FIG. 11 shows a flow chart explaining FIG. 9;
2 FIG. 12 shows a preferred variant of FIGS. 1 through 4
3 with an electronically commutated motor;
4 FIG. 13 is a circuit diagram analogous to FIG. 9, which
5 shows the electrical connections of a nonvolatile memory and
6 a serial data bus that serves to transfer electrical data
7 into or out of said memory;
8 FIG. 14 is a diagram explaining a start condition S and
9 a stop condition P for transfers via the serial bus;
10 FIG. 15 shows a typical data stream over the serial
11 bus;
12 FIG. 16 depicts the bus outputs of the transmitter
13 (FIG. 16a) and receiver (FIG. 16b), and of the clock signal
14 delivered by the master (FIG. 16c);
15 FIG. 17 shows an example of an instruction and data
16 word used to write an object over the serial bus;
17 FIG. 18 shows an example of an instruction and data
18 word used to read an object over the serial bus;
19 FIG. 19 shows an example of an object table permanently
20 stored in the device;
21 FIG. 20 is a schematic depiction of an arrangement
22 according to the present invention, its various memories,
23 and an exemplary depiction of data that are stored in said
24 memories;
25 FIG. 21 is a flow chart for interrogating a bus system
26 that connects a subordinate device (slave) to a main device
27 (master);
28 FIG. 22 is an overview showing how a fan 340 is
29 connected via a bus 13 to a laptop 11 in order to program
30 fan 340 in accordance with the requirements of an
31 application;
32 FIG. 23 shows a battery of fans with three fans, and
33 how they are controlled by a shared central unit 11 via a
34 serial bus 13; and
35 FIG. 24 is a view similar to FIG. 23, showing how

1 central unit 11 can be connected via a higher-performance
2 bus 346 to a server 344, in order to construct a more
3 extensive bus system.

4 **FIG. 1** illustrates a first embodiment of an arrangement
5 according to the present invention with which, in the
6 context of an electric motor 10, current limiting with
7 variable current limiting values I_{ref} is possible in program-
8 controlled fashion.

9 The arrangement has a microcontroller 12 that
10 communicates, optionally via a bus interface 13a and an
11 external bidirectional bus 13 that can be connected thereto,
12 with a computer 11 (FIG. 12) or another motor. What can be
13 used here is, for example, a (serial) I²C bus, or any other
14 known type of serial or parallel bus. (Regarding the I²C
15 bus, cf. for example Philips, IIC Peripherals, IC12 [Philips
16 Semiconductors company document, 1995].)

17 Connected to microcontroller 12, also via an (internal)
18 I²C bus 15, is a serial EEPROM 14, i.e. a nonvolatile
19 memory, in which data for the operation of motor 10 are
20 stored; these can be modified from outside via bus 13, data
21 traffic to and from EEPROM 14 being controlled by
22 microcontroller 12, which additionally controls functions of
23 motor 10, e.g. commutation thereof, as will be described
24 below with reference to FIG. 11. Microcontroller 12 thus has
25 the function of a master in relation to internal bus 15,
26 i.e. it controls transfers thereon; whereas in relation to
27 external bus 13 it has the function of a slave, i.e. data
28 transfer on external bus 13 is controlled by an external

1 device 11, e.g. by an ordinary desktop computer, a laptop,
2 or a special device (cf. FIG. 12 or 20).

3 Alternatively, it is also possible to use a
4 microcontroller or microprocessor having an integrated
5 EEPROM, which simplifies programming. Such microcontrollers
6 are available commercially.

7 Microcontroller 12 has an output A that can assume
8 three switching states, as explained in detail below with
9 reference to FIGS. 2 through 4. Connected to output A via a
10 high-resistance resistor 17 is a node 18 that is connected
11 via a resistor 20 to a regulated positive voltage V_{cc} , e.g.
12 +5 V, and via a resistor 22 to ground 24.

13 Node 18 is connected to positive input 26 of a
14 comparator 28 whose output 30 is connected via a resistor 32
15 (to establish the switching hysteresis) to input 26, also to
16 an input E of microcontroller 12 and, via a resistor 33, to
17 potential V_{cc} . Output 30 is also connected to an input 34 of
18 motor arrangement 10 (FIGS. 6 and 9 below show two examples
19 of a motor arrangement of this kind). A low signal at input
20 34 causes energy delivery to motor arrangement 10 to be
21 interrupted.

22 Motor arrangement 10 is in series with a low-resistance
23 measurement resistor 36 whose one terminal is connected to
24 ground 24. Motor current i results in a voltage u at
25 resistor 36 which is conveyed via a resistor 38 to negative
26 input 40 of comparator 28. Input 40 is connected via a
27 capacitor 42 to ground 24.

28 Resistor 38 forms, together with capacitor 42, a first-
29 order low-pass filter that, together with feedback resistor
30 32, determines the current limiting frequency, e.g. 15 to 20
31 kHz. This frequency is preferably above the highest
32 frequency that can be perceived by the human ear.

Typical component values

Microcontroller 12 COP 842 CJ (National Semiconductor)
(FIG. 10 shows, by way of example, the manufacturer's
terminal markings 1 through 20 of this microcontroller 12,
as well as the port designations used by the Applicant, e.g.
OUT1, OUT2, etc.)

EEPROM 14 two-wire serial CMOS EEPROM AT24C01A (ATMEL)

Resistor 22 47 k ohms

Resistors 17, 20, 33 100 k ohms

Resistor 32 1 M ohms

Resistor 36 1 ohm

Resistor 38 1 k ohms

Capacitor 42 22 nF

Capacitor 45 33 nF

Comparator 28 LM2901

Mode of operation

It will initially be assumed, for explanation purposes only, that
resistor 17 has a value of infinity (∞), so that the potential of output
A has no effect on the potential of node 18, which in this instance is
determined only by the ratio between resistors 20 and 22.

If current i in motor 10 rises, voltage u at measurement resistor
36 also rises; and if it exceeds the potential at positive input 26 of
comparator 28, the previously high output 30 of comparator 28 becomes
low, causing the current in motor arrangement 10 to be interrupted.

This causes voltage u to drop; negative input 40 of comparator 28
again becomes more negative than positive input 26, so that output 30 of
comparator 28 once again becomes high, and the current through motor
arrangement 10 is switched back on.

If motor current i therefore becomes so great that comparator 28
switches over, motor current i is continuously switched off and on in
the manner of a pulse-width modulation (PWM) system, causing motor
current i to be limited to a predefined value I_{ref} that is defined by the
potential at node 18.

1 Output A of microcontroller 12 is preferably a so-called tristate
2 output. **FIG. 2** shows the state $I_{ref} = 1$, in which output A is connected
3 via an internal switch 44 (transistor) to positive voltage V_{cc} , which is
4 filtered via a capacitor 45. This means that the high-resistance
5 resistor 17 (100 kW) is connected in parallel with resistor 20 (100
6 kW), thus causing the potential at node 18 to become higher; in other
7 words, in this case current limiting begins only at a higher value of
8 motor current i . This state is desirable while a motor is starting up,
9 since the motor current can in that context become very high for a short
10 period, and current limiting should therefore begin only at higher
11 current values in order to result in rapid acceleration of motor 10.

12 **FIG. 3** shows the state $I_{ref} = 0$, in which switch 44 (transistor) in
13 microcontroller 12 is nonconductive, and instead a switch 46, which
14 connects output A to ground 24, is conductive. This causes resistor 17
15 to be connected in parallel with resistor 22, so that the potential at
16 node 18 becomes lower; in other words, in this case current limiting
17 already begins when the current in motor 10 is lower. This state is
18 desirable if motor 10 is being decelerated or jammed by mechanical
19 influences, since the motor then cannot overheat due to electrical
20 losses.

21 **FIG. 4** shows the state $I_{ref} = TST$ (tristate). In this state both
22 internal switches 44, 46 of microcontroller 12 are nonconductive, so
23 that output A has a high resistance. In this instance resistor 17 has no
24 influence on the potential of node 18, i.e. said potential is lower than
25 when $I_{ref} = 1$ and higher than when $I_{ref} = 0$. This is a state that can be
26 used for normal operation of motor 10.

27 Switches 44, 46 in microcontroller 12 are transistors that are
28 controlled by the program of microcontroller 12, i.e. in this example
29 the value I_{ref} can be set, in program-controlled fashion, to three
30 different values: 0, 1, or TST.

31 **FIG. 5** shows, by way of example, a typical program sequence.

1 In step S50, motor 10 is initialized and started and begins its
2 acceleration, the duration T_s of which is taken from EEPROM 14, e.g.
3 3 seconds. This value can be entered from outside into EEPROM 14 via bus
4 13, microcontroller 12, and bus 15. Upon initialization (step S50) this
5 value, together with other values, is read out of EEPROM 14 into a RAM
6 in microcontroller 14.

7 Step S52 monitors whether the motor is still within acceleration
8 period T_s . If so, then in step S53 $I_{ref} = 1$ is set, i.e. switch 44 is
9 closed and switch 46 is opened. The program thereafter moves to step S56
10 (return) and begins another pass.

11 If it is found in step S52 that acceleration period T_s has
12 expired, the program goes to step S54, which checks whether motor
13 rotation speed n is below a predefined minimum rotation speed n_{min} . This
14 can mean that the motor is jammed, or that it is running too slowly. If
15 the answer in step S54 is Yes (Y), then in step S55 the motor is
16 switched off, e.g. by setting the two signals OUT1 and OUT2 in FIG. 9 to
17 zero. Rotation speed n_{min} is taken from EEPROM 14 upon initialization; it
18 can be modified via bus 13 by loading a different value for n_{min} into
19 EEPROM 14.

20 Step S57 then follows, in which the motor is de-energized for a
21 waiting time of, for example, 5 seconds. In the subsequent step S58, the
22 time T for acceleration (cf. S52) is reset to zero, and the program
23 proceeds via step S56 (return) back to the start (S50) and attempts to
24 restart the motor.

25 If the answer in step S54 is No (N), meaning the motor is
26 operating at a speed n in the normal range, the program then goes to
27 step S59. In this, the program continually checks whether current
28 limiting signals were present at input E during the entire duration of
29 the previous second (cf. FIG. 7), i.e. whether the current-limiting
30 function was active during the previous second. If so, the program goes
31 to step S60 which sets $I_{ref} = 0$, i.e. motor current i is, from now on,

1 limited to a lower value so that motor 10 is not excessively heated by
2 the motor current. The program then goes to step S56 (return).

3 If no current-limiting activity is ascertained in step S59, the
4 program goes to step S62, where $I_{ref} = TST$ is set, i.e. the current
5 limiting function is set to a value suitable for normal operation
6 (tristate; cf. FIG. 4).

7 **FIG. 6** shows a simple example of a motor arrangement 10, here
8 having a DC collector motor 70 that is connected in series with a power
9 MOSFET transistor 72 and drives, for example, a (symbolically indicated)
10 fan 73. A free-wheeling diode is labeled 74 and is connected
11 antiparallel with motor 70. Transistor 72 is controlled by an npn
12 transistor 75 and a pnp transistor 76, whose emitters are connected to
13 one another and to the gate of transistor 72. The collector of
14 transistor 75 is connected to Vcc, and that of transistor 76 to ground
15 24. The bases of transistors 75 and 76 are connected to one another and
16 to terminal 34 of FIG. 1 or 12.

17 If a low potential is present at input 34, transistor 75 is
18 inhibited and transistor 76 becomes conductive, so that MOSFET 72
19 becomes nonconductive and interrupts power to motor 70.

20 If input 34 has a high potential, transistor 75 then becomes
21 conductive and transistor 76 is inhibited, so that MOSFET 72 becomes
22 conductive and a current i flows to motor 70, as depicted at 78. The
23 depiction at 78 applies to the state in which current limiting is
24 effective. The circuit shown in FIG. 6 has the advantage that motor
25 voltage U_b is independent of voltage VCC.

26 **FIG. 7** shows the high current limiting value $I_{ref} = 1$ during the
27 period T_s , and then the limiting value $I_{ref} = TST$ in normal operation.

28 Motor 10 becomes jammed at time t , and one second later the
29 current limiting function switches to $I_{ref} = 0$ and thereby limits the
30 current in the motor (under program control) to a low value.

1 **FIG. 8** shows how the current limiting value I_{ref} can be switched
2 over, under program control by way of values in EEPROM 14, between its
3 three values as a function of time. This makes it possible, as depicted
4 in FIG. 8, to program a "soft start", i.e. one at low current.

5 If a microcontroller 12 having two tristate outputs A, A' is used,
6 as indicated in FIG. 1, it is then possible to generate more current
7 limiting values by also connecting output A' via a resistor 17" to node
8 18, resistor 17' usually having a resistance value different from that
9 of resistor 17. The number of limiting values equals three to the power
10 of the number of outputs; for example, with a microcontroller having two
11 tristate outputs A, A', $3^2 = 9$ different limiting values; with three
12 outputs A, A', and A", 27 different limiting values, etc.

13 It is a very advantageous feature of the invention that by way of
14 bus 13 and EEPROM 14, any desired states and times for controlling the
15 current limiting function can be defined for microcontroller 12. The
16 data transferred via serial bus 13 are stored in EEPROM 14 and remain
17 stored there, and available for subsequent motor operation, even after
18 voltage Vcc has been switched off. As a result, it is possible to
19 program a motor optimally for its particular operating task without
20 needing to modify resistors or other electrical elements in said motor's
21 circuitry.

22 **FIG. 9** shows, as a variant of FIG. 6, an embodiment having a
23 collectorless DC motor 10' that is preferably used to drive fans.
24 DE 23 46 380 C3 describes a typical example of the mechanical
25 configuration of such motors. Parts that are identical or functionally
26 identical to those in the previous Figures are labeled with the same
27 reference characters as therein, and usually are not described again.
28 External bus 13 and its interface 13a are not depicted in FIG. 9 but are
29 shown in FIG. 13. EEPROM 14 and its bus 15 are only schematically
30 indicated in FIG. 9 (see FIG. 13 for details).

1 Motor 10' has two winding phases 90, 92, each connected at one
2 terminal to a positive lead 94 at, for example, 48 volts. A permanent
3 magnet rotor is indicated symbolically at 96. When it rotates, it
4 controls with its magnetic field a Hall generator 98 that is depicted
5 once again on the extreme left of FIG. 9. Be it noted that the current
6 limiting function can be used with any type of collectorless DC motor,
7 i.e. not only with a two-phase motor but also with a motor having one
8 phase, three phases, etc.

9 The other terminal of phase 90 is connected via an npn Darlington
10 transistor 100 to a node 102, and the other terminal of phase 92 is
11 connected via an npn Darlington transistor 104 to node 102. Current
12 measurement resistor 36 that has already been described is located
13 between node 102 and ground 24.

14 Free-wheeling diodes 100', 104' are located antiparallel to the
15 two Darlington transistors 100, 104. When transistor 100 conducts, a
16 current i_1 flows. When transistor 104 conducts, a current i_2 flows. Both
17 currents are limited, by the current limiting arrangement already
18 described, to a (variable) value I_{ref} .

19 Output G1 of microprocessor 12, whose terminals and terminal
20 markings are depicted in detail in FIG. 10, leads to terminal 106 of an
21 AND element 108 whose output is connected via a resistor 110 to the base
22 of transistor 100.

23 Output G2 of microprocessor 12 leads to input 112 of an AND
24 element 114 whose output is connected via a resistor 116 to the base of
25 transistor 104.

26 The second input 118 of AND element 108 and the second input 120
27 of AND element 114 are connected via a resistor 122 (e.g. 100 kW) to
28 positive voltage V_{cc} , and also to input E of microprocessor 12 and to
29 output 30 of comparator 28.

1 When output 30 of comparator 28 is low, it inhibits both AND
2 elements 108, 114 and thus prevents signal OUT1 =1 (at port G1) from
3 activating transistor 100, or signal OUT2 = 1 (at port G2) from
4 activating transistor 104. When current limitation is engaged,
5 therefore, the transistor 100 or 104 that is presently conductive is
6 inhibited by the signal at output 30 of comparator 28, and that signal
7 is analyzed in microprocessor 12 via input E (cf. step S58 of FIG. 5).

8 FIG. 9 shows at 124 a quartz oscillator that is connected to
9 terminals CK0 and CK1 of microprocessor 12 and defines its clock
10 frequency, for example 4 MHz. Reset input Res is connected via a
11 capacitor 126 to ground 24, and via a resistor 128 to +Vcc. These two
12 component generate a power-up reset at startup time, in the usual way.

13 Hall generator 98, for example of the type HW101A, is connected
14 for power supply purposes via a resistor 130 (e.g. 3.3 k ohms) to +Vcc,
15 and directly to ground 24. Its output signal u_H is conveyed to the two
16 inputs of a comparator 132 (e.g. LM2901D) whose Vcc input has associated
17 with it a filter capacitor 134 of, for example, 33 nF. Its output is
18 connected via a feedback resistor 135 (e.g. 100 k ohms) to the positive
19 input, and via a so-called pull-up resistor 136 (e.g. 33 k ohms) to
20 +Vcc, and directly to the INT port (FIG. 10) of microprocessor 12,
21 resulting at the latter, during operation, in a HALL signal that is
22 controlled by rotor magnet 96. This signal therefore always has the
23 value HALL = 0 during one rotor rotation of 180° el., and the value HALL
24 = 1 during the subsequent rotation of 180° el.

25 FIG. 11 shows the manner in which motor 10' is commutated by
26 microprocessor 12. At step S140, motor 10' is started, i.e. switched on,
27 initialized with values from EEPROM 14, etc.

28 In step S142, the Hall port INT is interrogated. If the signal
29 there equals "0", the program proceeds to step S144 and OUT1 = 1 and
30 OUT2 = 0 are set, i.e. transistor 100 is switched on and transistor 104
31 is switched off, so that a current i_1 flows in winding phase 90. This
32 state in step S144 is stored until a change in the HALL signal is
33 detected.

1 The program then goes to step S146, where, for example, the
2 routine according to FIG. 5 is executed, and the program then proceeds
3 via loop S148 back to step S142.

4 If it is ascertained in S142 that $HALL = 1$, the program then goes
5 to step S150, where $OUT1 = 0$ (transistor 100 switched off) and $OUT2 = 1$
6 (transistor 104 switched on) are set, so that a current i_2 now flows
7 through phase 92.

8 The result, when current limiting is engaged, is then that when
9 the current i through measurement resistor 36 becomes too high, the
10 particular transistor that is conductive (100 or 104) is inhibited.

11 By (internally) switching over output A of microcontroller 12, the
12 current limiting value I_{ref} can be switched over in program-controlled
13 fashion to three different current limiting values I_{ref} , as already
14 described in detail.

15 If it is assumed that in FIGS. 1 through 4 the two resistors 17
16 and 20 have a value of 100 k ohms and resistor 22 a value of 47 k ohms,
17 and that voltage V_{cc} is about +5 V, then node 18 has a potential of
18 2.5 V in FIG. 2, 1.6 V in FIG. 4, and 1.24 V in FIG. 3.

19 These are relatively high voltages, and measurement resistor 36
20 through which motor current i flows must also be correspondingly large
21 so that voltage u at this resistor is greater than the aforesaid
22 potentials (1.24, 1.6, or 2.5 V), and the current limiting function is
23 thereby activated.

24 As a result, corresponding losses in resistor 36 always occur
25 during operation; this is undesirable, since it reduces the efficiency
26 of the motor. If, on the other hand, resistor 22 is made substantially
27 smaller than resistor 20, this has only a very minor effect when, in the
28 state shown in FIG. 3, the high-resistance resistor 17 is connected in
29 parallel with the low-resistance resistor 17. (Resistor 17 must have a
30 high resistance, since the currents through microcontroller 12 must not
31 exceed a specific, very low value.)

The circuit depicted in **FIG. 12** offers some improvement here, since in it, the losses in measurement resistor 36 become smaller, i.e. measurement resistor 36 can be given a lower resistance value. Parts that are identical or functionally identical to those in the previous Figures are labeled in FIG. 12 with the same reference characters, and usually are not described again.

In this case node 18 is connected to positive input 26 of comparator 28 not directly, but via a second, high-resistance voltage divider 160. The latter contains a first resistor 162 between node 18 and positive input 26 of comparator 28, as well as a second resistor 164 between positive input 26 and ground 24. The tapping point of this second voltage divider 160 is labeled 163, and is connected directly to positive input 26. If, for example, resistor 162 is given a value of 1 M ohms, and resistor 164 a value of 100 k ohms, the potential at positive input 26 is then only approximately one-eleventh of the potential at node 18, and the value of measurement resistor 36 can therefore be reduced to approximately one-tenth of that in FIGS. 1 through 4; the same is true of the losses at that resistor, correspondingly improving the motor's efficiency. Since resistors 162, 164 together have, for example, a value of 1.1 M ohms, while resistor 22 has a value, for example, of only 47 k ohms, voltage divider 160 has little influence on the magnitude of the potential at point 18.

Examples of values for FIG. 12

Microcontroller 12	COP 842 CJ (National Semiconductor)
(FIG. 10 shows, by way of example, the manufacturer's terminal markings 1 through 20 of this microcontroller 12, as well as the port designations used by the Applicant, e.g. OUT1, OUT2, etc.)	
EEPROM 14	two-wire serial CMOS EEPROM AT24C01A (ATMEL)
Resistor 22	47 k ohms
Resistors 17, 20, 33, 164	100 k ohms
Resistor 32	1 M ohms
Resistor 36	0.1 ohm
Resistor 38	1 k ohms
Capacitor 42	22 nF
Comparator 28	LM2901
Resistor 162	1 M ohms
Resistor 164	100 k ohms

1 The mode of operation is the same as described in FIG. 1, but in
2 this embodiment resistor 36 can have a much lower value, since the high-
3 resistance voltage divider 160 causes the adjustable comparison voltages
4 at position input 26 to be substantially reduced (in this example, to
5 values of approximately 0.12, 0.16, or 0.25 V), so that current limiting
6 engages when the voltage u at measurement resistor 36 exceeds the low
7 voltage at positive input 26 established by microcontroller 12.

8 **FIG. 13** supplements the depiction of FIG. 9, i.e. certain features
9 of FIG. 13 are not (or only schematically) depicted in FIG. 9 for lack
10 of space, and conversely certain features of FIG. 9 are not depicted in
11 FIG. 13. FIG. 9 concerns substantially the motor portion, and FIG. 13
12 the interface 13a for the bus connection as well as the connections of
13 EEPROM 14. Parts that are identical or functionally identical to those
14 in previous Figures are labeled with the same reference characters as
15 therein, and usually are not described again.

16 EEPROM 14 receives at its data input (SDA) 190 the signal ESDA
17 from port L3 (cf. FIG. 10) of microcontroller 12. Its clock input (SCL)
18 192 similarly receives the clock signal ESCL from port L4 (FIG. 10) of
19 microcontroller 12. Input 190 is connected via a resistor 196 to Vcc,
20 and input 192 via a resistor 194.

21 Write-protect input (WP) 198 of EEPROM 14 is connected via a lead
22 CS (= chip select) to port L0 (FIG. 10) of microcontroller 12. Only when
23 the signal at L0 is high can data be written into EEPROM 14.

1 If said signal is low, EEPROM 14 is write-protected. Terminals VSS, AD,
2 A1, and A2 of EEPROM 14 are connected to ground 24, and input VCC to
3 voltage Vcc, as depicted.

4 Lines ESDA and ESCL thus constitute serial bus 15 of EEPROM 14,
5 over which data traffic flows from and to EEPROM 14. Normally, EEPROM 14
6 (built into the motor) is programmed once at the factory (via serial bus
7 13), and its terminal 198 then remains at a low potential for the entire
8 operating life of the motor; but in principle, reprogramming of EEPROM
9 14 is possible at any time if the write protection is cancelled.

10 FIG. 13 also shows details of bus interface 13a to external bus 13
11 (FIG. 1). A data line 210 (DATA), which is connected via a resistor 212
12 to port SI (FIG. 10) of microcontroller 12, leads to interface 13a. From
13 port SI a resistor 214 also leads to Vcc, and a capacitor 216 goes to
14 ground 24. Port SI is also connected to the emitter of a pnp transistor
15 220, whose collector is connected to ground 24 and whose base is
16 connected via a resistor 222 to port SO (cf. FIG. 10) of microcontroller
17 12.

18 Interface 13a furthermore has a clock line (CLOCK) 226 that is
19 connected via a protective resistor 228 to port SK (FIG. 10) of
20 microcontroller 12. The latter is also connected via a resistor 230 to
21 Vcc, and via a capacitor 232 to ground 24.

22 Bus interface 13a is regularly interrogated in microcontroller 12
23 to determine whether there is any signal change in it (slave mode);
24 if so, the corresponding procedures are initiated in microcontroller 12,
25 as will be described below with reference to FIGS. 14 through 18.

26 For serial data transfer, microcontroller 12 that is used in the
27 exemplary embodiment (COP 842 CJ) has a serial interface with a clock
28 line SCL (serial clock), a data input line SI (serial in), and

1 a data output line SO (serial out). This is therefore a three-line
2 system, whereas an I²C bus operates with only two lines, namely line 210
3 for data (SDA) and line 226 for the clock signal (SCL).

4 Conversion of the three-line system (SO, SI, and SCL) to the two-
5 line system 210, 226 is provided by pnp transistor 220, which connects
6 data output SO via a collector circuit to line 210 for the data. The pnp
7 transistor 220 is therefore used so that the output signals at port SO
8 are not inverted.

9 Data input SI is connected directly, via protective resistor 212,
10 to data line 210. Pull-up resistors 214, 230 ensure that a defined
11 voltage level is present at all times on lines 210, 226.

12 In this fashion, it is possible herein, very advantageously, to
13 implement an I²C bus in slave mode.

14 Typical values for FIG. 13

15 Microcontroller 12 COP 842 CJ (National Semiconductor)
16 (FIG. 10 shows, by way of example, the manufacturer's terminal markings
17 1 through 20 of this microcontroller 12, as well as the port
18 designations used by the Applicant, e.g. OUT1, OUT2, etc.)

19 EEPROM 14 two-wire serial CMOS EEPROM AT24C01A (ATMEL)

20 Transistor 220	BC856B
21 Resistor 194, 196	22 k ohms
22 Resistors 214, 230	47 k ohms
23 Resistor 222	100 k ohms
24 Resistors 212, 228	47 ohms
25 Capacitors 216, 232	33 nF

26 Mode of operation of FIG. 13

27 Data transfer on internal bus 15 takes place in accordance with the
28 protocol of the I²C bus, as described in the reference cited initially,

1 microcontroller 12 being the master and EEPROM 14 the slave. New data
2 can be stored in EEPROM 14 only if the signal on line CS is high. If
3 this signal is low, it is possible only to transfer stored data out of
4 EEPROM 14 to microcontroller 12. This occurs principally during
5 initialization after the motor is switched on, when the necessary data
6 are transferred out of EEPROM 14 into RAM 330 (FIG. 20) in
7 microcontroller 12.

8 **FIG. 14** shows, for the protocol of an I²C bus, the start condition
9 at S and the stop condition at P. The start condition S exists when data
10 line (SDA) 210 changes from high to low while clock line (SCL) 226 is
11 simultaneously high. The communication buffers (buffer memories 332 in
12 FIG. 20) are then erased, and communication is switched to active
13 status. The byte counter is reset. (Communication buffers 332 and the
14 byte counter are located in RAM 330 of microcontroller 12.)

15 The stop condition P (FIG. 14) exists when data line (SDA) 210
16 changes from low to high while clock line (SCL) 226 is simultaneously
17 High. In the case of a write access to microcontroller 12, the data are
18 written into the relevant communication buffer 332 (FIG. 20). After the
19 stop condition, the communication status is deactivated. Only now can
20 data be written into RAM 330 or EEPROM 14.

21 **FIG. 15** shows the bit stream during a transfer on the I²C bus. The
22 symbols denote:

23 MSB = most significant bit
24 LSB = least significant bit
25 A = acknowledgment
26 S = start condition
27 P = stop condition.

28 An acknowledgment from the receiver occurs at 400 and at 402. At 404 the
29 byte has been completely transferred.

FIG. 16 shows, at a) the data 410 generated by the transmitter,
 and at b) the data 412 generated by the receiver. In **FIG. 16**,
 HIGH = no acknowledge; and
 LOW = acknowledge.
FIG. 16c) shows clock signal SCL 414 from the master, the ninth
 clock pulse 416 being the clock pulse for acknowledgment A.
 In the "receive" communication mode, the corresponding data bit
 is received (i.e. read in) from data line (SDA) 210 after the rising
 edge on clock line (SCL) 226.
 In the "transmit" communication mode, the next bit on data line
 210 is output (via transistor 220) after a falling edge on clock line
 (SCL) 226.
FIG. 17 shows the "write object" communication sequence 420. Here,
 as in **FIG. 18**:
 S = start condition (cf. **FIG. 14**)
 P = stop condition (cf. **FIG. 14**)
 black areas: from master to slave
 white areas: from slave to master
 A = acknowledgement (data line SDA 210 low)
 A/ = no acknowledgment (data line SDA 210 high)
 A complete communication, in which one object is sent to the
 slave, comprises a start condition "S" 240, after which eight bits 242
 are received, optionally acknowledged with an acknowledgement signal A
 244. These eight bits 242 are made up of seven slave address bits and
 one read/write bit 243, which here has a value of 0 (for "write"). If
 slave address 242 matches the device address (324 in **FIG. 20**),
 acknowledgment A is sent, and object address 246 is then received and
 acknowledged at 247. Object table 280 in **FIG. 19** contains (in column
 286) a datum regarding the object length associated with object

1 address 246. This indicates how many data blocks (bytes) need to be
2 transferred.

3 The corresponding number of data blocks 248, 249, and stop
4 condition "P" 250, are then transferred. The data are then received into
5 the particular memory obtained from object table 280 and indicated
6 therein in columns 288, 290 (FIG. 19).

7 Address 324 of a device (FIG. 20) can be assigned without
8 restriction within a bus system by master 11 (FIG. 20), and is then
9 stored in nonvolatile fashion in EEPROM 14 of the relevant motor 10 or
10 10'.

11 **FIG. 18** shows the "read object" communication sequence. This
12 sequence is described in more detail below in conjunction with FIG. 20.
13 Parts in FIG. 18 that are identical to FIG. 17 are given the same
14 reference characters as in that Figure.

15 **FIG. 19** shows, by way of example, an object table 280 permanently
16 stored in ROM 336 (FIG. 20) of microcontroller 12, preferably as a
17 hardware component of microcontroller 12.

18 The meanings of the respective fields are as follows:

19 AA Object address

20 BB Object name

21 CC Number of bytes

22 DD Memory medium

23 EE Hardware address

24 and the meanings of the fields in column 284 (Object name) are:

25 B1 Control word init

26 B2 Status word

27 B3 Setpoint speed

28 B4 Actual speed

29 B32 Manufacturer

30 B33 Software version

Object table 280 contains (in this graphical depiction) a column 282 with object addresses, a column 284 with object names, a column 286 with the length of the object in question (1 or 2 bytes), a column 288 identifying the memory medium (here: RAM, ROM, or EEPROM), and lastly a column 290 with the hardware address.

For example, the software version used in the device has the object address "33", the object name "software version" (field B33), and a length of one byte. It is located in the ROM (336) of microcontroller 12, and has the hardware address "0x01" in ROM 336. The hardware addresses are preferably indicated in the form of a hexadecimal word.

The instantaneous rotation speed derived from the "Hall" signal has the object address "04" and the object name "Actual speed" (field B4); it has a length of two bytes, is located in RAM 330 (of microcontroller 12), and has therein the hardware address "0x01", again in the form of a hexadecimal word.

The general procedure is to store the first object in EEPROM 14 under the address "0x00" therein, the second object under "0x01", etc. The same procedure is used in RAM, i.e. there as well, the first object has the hex address "0x00", the second object "0x01", etc. Object table 280 can begin in ROM 336 at a suitable, defined address.

When the hardware address of an object is read from object table 280, what is read is a hexadecimal word, and along with it the information as to whether that object is stored (or to be stored) in RAM 330, ROM 336, or EEPROM 14. Also evident from object table 280 is the length of the addressed object.

FIG. 20 shows, in highly schematic form, the distribution of various objects to the memories present in the device (fan).

The meanings of the labels used are indicated in the following list:

1	A1	Buffer A
2	A2	Buffer B
3	A3	Buffer C
4	A4	Buffer D
5	A5	Buffer E
6	A6	Buffer F
7	A10	Status word
8	A11	Actual speed
9	A12	I_{ref}
10	A13	Operating hours
11	A14	Device address
12	O1	Manufacturer
13	O2	Software version
14	O3	Object table
15	X1	Device address
16	X2	Setpoint speed
17	X3	Operating hours
18	X4	Factory number
19	X5	Init control word
20	X6	I_{ref} start
21	Y1	Processor

EEPROM 14 contains the address (X1) 324 of the device, the setpoint speed (X2), operating hour count (X3), factory number (X4), init control word (X5), current limiting value I_{ref} for startup (X6), and additional data.

When motor 10 starts up and at each reset, an initialization occurs, during which various data are transferred via I²C bus 15 from EEPROM 14 into RAM 330 of microcontroller 12: for example, as indicated, the number of operating hours (A13), address 324 of the device (A14), and the current limiting value I_{ref} for startup (A12). These are for the most part the values that the motor needs before starting up. RAM 330 also contains buffer memories (communication memories) 332, for

1 example called buffer A (A1) through buffer E (A6), each of which can
2 store one byte. Also located therein is a status register 334 that
3 contains the present values SDA and SCL (on lines 210 and 226,
4 respectively), as well as the values SDA-A and SCL-A obtained during the
5 previous interrogation.

6 During operation, lines 210, 226 of I²C bus 13 are continually
7 interrogated, e.g. every 0.5 ms or every 1 ms, to determine whether
8 there are any signal changes on them. Such changes in this case arrive
9 via bus 13 from a computer 11 that functions as master and, for example,
10 regularly performs an interrogation of the actual speed in RAM (330) of
11 microcontroller 12. The number of interrogations per second determines
12 the transfer rate on bus 13, e.g. 1000 Bd. This is based on the needs of
13 the application. If, for example, the device is programmed only once in
14 its lifetime, the transfer rate is immaterial. For an application in a
15 control system, a transfer rate of 1000 Bd is sufficient in most cases,
16 although the number of devices connected to bus 13 of course plays an
17 important role. Data transfer from and to the device takes place via bus
18 13, i.e. by way of the two lines 210, 226 of FIG. 13.

19 **FIG. 21** shows the procedures for an interrogation of these lines.
20 Step S300 is the start. In step S302, the instantaneous values SDA and
21 SCL on lines 210, 226 are read, and in step S304 are compared to the
22 values SDA-A and SCL-A in status memory 334, which were stored during
23 the previous pass. In step S304, SDA is therefore compared to SDA-A, and
24 SCL to SCL-A.

25 As FIG. 14 shows, a change in the value SDA from "1" to "0" means
26 a start condition if the value SCL simultaneously retains a value of
27 "1". In step S304 changes of this kind are detected, analyzed, and
28 conveyed to a branching table S306 which, for example when a start
29 condition "S" is detected, proceeds to step S308 which triggers the
30 "start condition" function in the program. Similarly, the program can go
31 from branching table S306 to the stop condition "P" (S310), which is
32 also explained in FIG. 14, or to an acknowledgment "A" (S312) that is
33 explained in FIG. 16b, or to "send byte" in S314 or to "receive byte" in
34 step S316. Steps S310 through S316 trigger the respective corresponding

1 sequences in processor 12, i.e. the corresponding functions are called
2 therein.

3 The program then goes to step S318, where the values of SDA-A and
4 SCL-A in status register 334 are updated. A return occurs in step S320,
5 i.e. completion of this routine.

6 The meanings of the labels in FIG. 21 are therefore:

7 S304 "Compare SDA to SDA-A, compare SCL to SCL-A"

8 S306 "Branching table"

9 S308 "Start condition S"

10 S310 "Stop condition P"

11 S312 "Acknowledgment A"

12 S314 "Send byte"

13 S316 "Receive byte"

14 If, in FIG. 20, PC 11 wishes to inquire as to the actual speed, it
15 then, as shown in FIG. 18, opens communication with start condition 240
16 (FIG. 18 concerns operation 422, i.e. "read object"). The subsequent
17 first byte 242 contains the address of the addressed device in bits 1
18 through 7, and a "0" for "write" in bit 8 (least significant bit 243).

19 Bits 1 through 7, i.e. the address, are compared in
20 microcontroller 12 to address 324 in RAM 330. If bits 1 through 7 in
21 portion 242 match address 324, bit 8 is then checked. If the address
22 does not match, microcontroller 13 disconnects itself from the
23 communication on bus 13. (Other devices with other addresses can be
24 connected to bus 13, for example twenty other devices that operate in
25 parallel with the device depicted in FIG. 20 and can be separately
26 switched on or off, or otherwise controlled, by PC 11 as necessary.)

27 Once address 242 has been checked and bit 243 (for "write") has
28 been checked, microcontroller 12 sends the acknowledgment signal "A"
29 (244 in FIG. 18). After receiving signal 244, PC 11 sends object address
30 246, in this case e.g. (as shown in FIG. 19) object address "04" (actual
31 speed), this being the address of the object that PC 11 wishes to read

1 next. Following the acknowledgment signal "A" 247 (from microcontroller
2 12), PC 11 sends a stop condition "P" that is labeled 250 in FIG. 18.

3 Based on object address 246, a determination is then made from
4 object table 280 that the object, in this case e.g. the actual speed,
5 comprises two bytes; in microcontroller 12, the two bytes of the actual
6 speed are then transferred into the corresponding buffer memories 332 so
7 they are ready there for a subsequent transfer.

8 PC 11 then sends (as shown in FIG. 18) another start condition
9 252, and the first byte 254 with the same device address as in byte 242,
10 but with a value of "1" (for "read") in bit 8 that is labeled 256. Once
11 the address and bit 8 have been checked, PC 11 waits for the transfer of
12 data blocks 258, 262 from the corresponding buffers in buffer memories
13 332, and they are transferred successively via I²C bus 13 to PC 11.
14 After byte 258, the latter sends an acknowledgment "A" that is labeled
15 260 in FIG. 18 and is checked by microcontroller 12. After the last byte
16 262, it sends (at 263) no acknowledgment ("A/"). When PC 11 has received
17 both data bytes 258 and 262, it sends the stop condition "P" 264. This
18 means that the number of transferred data bytes 258, 262 has been
19 checked and is correct.

20 Writing to EEPROM 14

21 This is procedure 420 in FIG. 17, namely "write object". PC 11,
22 which constitutes the master, opens communication with the start
23 condition "S" 240 (cf. FIG. 17). The next byte 242 contains the device
24 address in its bits 1 through 7, and contains in the least significant
25 bit 243 (bit 8) a datum as to whether a read or a write operation is to
26 follow. In this case bit 8 is a zero, i.e. computer 11 wishes to write
27 data, for example into RAM 330 or EEPROM 14. The location to which
28 writing is to occur is determined from object address 246 and object
29 table 280.

30 First the address in bits 1 through 7 is compared to device
31 address 324 in RAM 330 of microcontroller 12. If these seven transferred
32 bits do not match device address 324, the device disconnects itself from
33 communication. If the address does match, bit 8 is checked.

1 Microcontroller 12 then sends an acknowledgment signal "A" 244.

2 PC 11 then sends the next byte 246, namely the object address.
3 Based on this address, information is retrieved from object table 280
4 regarding the object that is to be transferred next. If the object is,
5 for example, the setpoint speed (table value B3 in column 284, "Object
6 name"), it is apparent from the object address "03" that the setpoint
7 speed contains two bytes and is stored in EEPROM 14 under the address
8 "0x01". This therefore means that two bytes need to be transferred; and
9 if, for example, more or fewer than two bytes were transferred, this
10 means an error has occurred. After byte 246 is received, there is
11 another acknowledgment signal "A" that is labeled 247. Data bytes 248,
12 249 of that object are then transferred from PC 11 into the associated
13 buffers 332 in RAM 330, an acknowledgment signal "A" being sent by
14 microcontroller 12 after each byte.

15 Once PC 11 has transferred all the bytes and obtained an
16 acknowledgment signal "A" each time, it sends the stop condition "P"
17 250. A check is then made in microcontroller 12 to determine whether the
18 expected number of bytes has been transferred. If this number does not
19 match, the data are discarded. If the number matches, the data are
20 written into EEPROM 14 at the identified address "0x01", by calling the
21 transfer routine of I²C bus 15 to the EEPROM. This routine first needs
22 the address ("0x01") into which the data are to be stored in EEPROM 14.
23 The routine then transfers the data that were stored, upon reception
24 from PC 11, in data buffers 332 in RAM 330. The routine sends the data
25 from buffer 332 with data byte 248, and then from buffer 332 with data
26 byte 249, to EEPROM 14. Based on the number of bytes in the object,
27 which was determined from column 286 of object table 280, the routine
28 knows which buffers 332, and how many of them, need to be read out and
29 transferred.

30 After the transfer into EEPROM 14, the transferred data can
31 optionally be read back again in order to make a comparison with the
32 transmitted data and thereby check for a correct transfer.

Outputting data from EEPROM 14

This transfer also takes place via buffer memories 332 in RAM 330 of microcontroller 12, i.e. a first instruction (FIG. 18, above) of PC 11 (master) causes the data to be transferred out of EEPROM 14 into the relevant buffer memories 332, and a second instruction (FIG. 18, below) causes these data to be transferred out of the relevant buffer memories 332 to PC 11.

This transfer is thus initiated by PC 11, which functions as master. After the start condition "S" 240, it sends the first byte 242 with the device address, and bit 243 which in this case contains a zero, i.e. denoting a write instruction. Once the address in byte 242 has been successfully checked, bit 243 is checked. Microcontroller 12 then sends (at 244) an acknowledgment signal "A". PC 11 thereupon transfers, in byte 246, the object address of the object that it then wishes to read out. The transfer is acknowledged by microcontroller 12 with an acknowledgment signal "A" 247, and PC 11 then sends, at 250, a stop condition "P".

The object in question, how long it is, and where it is stored are determined from object table 280 (FIG. 19) by way of the object address (byte 246). If the object address is, for example, "03", the object is then B3 "setpoint speed" with a length of two bytes, and it is stored in the EEPROM at the address "0x01". With the help of these data, that object, i.e. in this case the setpoint speed, is transferred from EEPROM 14 into the corresponding buffers 332 of RAM 330.

PC 11 then once again sends a start condition "S" at 252, and then at 254 sends the first byte with the device address and bit 256, which in this case has a value of "1" corresponding to a read operation. Once again, the device address (in byte 254) is compared to address 324 in RAM 330, and if they match, bit 256 is checked. Once the check is successfully completed, microcontroller 12 sends (at 257) an acknowledgment signal "A". It then transmits the data out of buffer memories 332 in RAM 330. First comes the first byte 258 that is acknowledged (at 260) by PC 11 with an acknowledgment signal "A".

1 Then comes the second and last byte 262, for which no acknowledgment
2 ("A/" at 263) is made prior to the subsequent stop condition 264. Since
3 in this case the transferred object contains two bytes 258, 262, the
4 stop condition "P" is sent by PC 11 at 264 because PC 11 has received
5 two bytes.

6 During operation, the motor therefore operates with the data that
7 were stored in RAM 330 of microcontroller 12 at initialization. After a
8 reset, for example as a result of electromagnetic interference, these
9 data are lost. For that reason, RAM region 330 is reinitialized at each
10 reset and after the device has started up, i.e. the data that are to be
11 used for operation are loaded from EEPROM 14 via bus 15 into RAM region
12 330 of microcontroller 12.

13 During operation, as just explained, data can be read out from
14 EEPROM 14 or conversely written into EEPROM 14. There also exists the
15 possibility of reading out data from RAM 330, i.e. for example the
16 actual speed (object A11 in FIG. 20) or from ROM 336 (e.g. the
17 manufacturer, object O1 in FIG. 20), or writing such data into RAM 330,
18 e.g. the desired setpoint speed as defined by master 11. The location to
19 which the data are written or from which they are retrieved (RAM 330,
20 ROM 336, or EEPROM 14, and the address therein) is ascertained from
21 object table 280, which is permanently stored in the device. The use of
22 this object table thus eliminates the need to transfer detailed address
23 data in a write or read instruction, i.e. a kind of indirect addressing
24 is used here, since all the essential data for the objects are stored in
25 object table 280, preferably in the form of a permanent memory (ROM).

26 Because buffer memories 332 are interposed, the result in each
27 instance is that when data are read, they are read out from said buffer
28 memories 332, and when data are written, they are written first into
29 said buffer memories 332, so that corresponding address indications can
30 be omitted from the instructions. The overall result is that the
31 instructions are of simple configuration and are rapidly executed, so
32 that it is possible to work with a simple, economical microcontroller
33 that can additionally handle other tasks such as:

1 A/D conversion,
2 current limiting,
3 speed regulation,
4 controlling commutation of motor 10' (FIG. 11),
5 and others.

6 If the quantity of data that needs to be transferred over bus 13
7 or 15 during a transfer is greater than the number of buffer memories
8 332, the transfer is divided into a plurality of transfers, i.e. into
9 packets.

10 **FIG. 22** shows the manner in which an equipment fan 340 is
11 connected via its interface 13a and serial bus 13 for programming on a
12 laptop 11. In this fashion, the data in EEPROM 14 of fan 340 can be
13 adapted to specific conditions. Fan 340 is then disconnected from bus 13
14 and operated as an independent unit, since the data that were input
15 remain stored in EEPROM 14. Operating hours are continuously counted in
16 EEPROM 14, and can be read out by once again connecting laptop 11.

17 **FIG. 23** shows a "battery" of fans with three equipment fans 340A,
18 340B, 340C, each of which has its own EEPROM 14A, 14B, 14C that (in the
19 fan) is connected in each case via a serial bus 15 to the
20 microcontroller therein.

21 All three fans are connected via bus 13 to a central unit 11, e.g.
22 a PC. Stored in EEPROM 14 is, for example, the address A of fan 340A,
23 also the value I_{ref} for current limitation at startup, and the time T_{SA}
24 (cf. FIG. 5, step S52), i.e. the time T_s for fan 340A.

25 EEPROMs 14B and 14C analogously contain the (device) addresses B
26 and C of fans 340B and 340C, respectively. They also contain the
27 associated values I_{ref} for current limitation for the particular fan, and
28 times T_{SB} and T_{SC} . This makes it possible to stagger the starting times
29 for the three fans, i.e. fan 340A is started, for example, at maximum
30 current, fan 340B at medium current, and fan 340C at low current,

1 so as not to overload a central power supply (not shown) for all three
2 fans during startup. Alternatively, the fans can be switched on at
3 staggered times in the same fashion.

4 Because central unit 11 continuously monitors the rotation speeds
5 of all three fans, it is possible to detect if, for example, fan 340B is
6 jammed; central unit 11 can then, via bus 13, correspondingly increase
7 the speeds of fans 340A and 340C to compensate for this failure. For
8 that purpose, in such a case a higher setpoint speed for fans 340A, 340C
9 is defined via bus 13, as already described above in detail.

10 At low temperatures, central unit 11 can switch off one or more of
11 the fans via bus 13.

12 The depiction in **FIG. 24** is similar to that of FIG. 23. Since bus
13 13, in the very simple and economical design described, needs to be only
14 relatively short (e.g. a maximum of 4 meters long), central unit 11 can
15 be connected via a higher-performance bus 346 to a server 344. As
16 indicated, this can be, for example, a CAN bus or a LON bus or an
17 Interbus-S. Communication is also possible, by way of any desired bus
18 348, with a central unit 11A that optionally controls further fans, and
19 via a bus 350 with a central unit 11B that also can control additional
20 fans or other devices. The EEPROMs of the three fans 340A, 340B, 340C of
21 FIG. 24 can be identical to those of FIG 23, and are therefore not
22 depicted again in FIG. 24.

23 The invention is of course not limited to being applied to fans,
24 but this is a very advantageous field of application since with fans
25 there are numerous variables that need to be adjusted depending on the
26 particular application.

27 It must be pointed out once again that there are many different
28 bus systems, and that the serial bus described therefore represents only
29 one preferred embodiment of the invention. In other respects as well,
30 many variants and modifications are possible within the scope of the
31 present invention.

Claims

1. An arrangement having an electric motor (10; 10'),
having a microcontroller (12) or microprocessor, hereinafter
simply called a microprocessor, for influencing at least one motor
function, in which arrangement
an output (A) of the microprocessor (12) can be switched over in
program-controlled fashion to a high level or to a low level;
and a tapping point (19) [sic] of a first voltage divider (20, 22)
is connected to that terminal via a resistor (17) in order to make the
potential of that voltage divider tapping point (18) switchable in
program-controlled fashion between at least two values by modifying that
level.
2. The arrangement as defined in claim 1, in which said resistor (17)
is of high-resistance configuration.
3. The arrangement as defined in claim 2, in which the value of said
resistor (17) is 50 kilohms or more.
4. The arrangement as defined in one or more of claims 1 through 3,
in which said output (A) of the microprocessor (12) can be switched over
in program-controlled fashion to a third, high-resistance state (FIG.
4).
5. The arrangement as defined in one or more of the foregoing claims,
in which the potential at the tapping point (18) of the first voltage
divider (20, 22) serves to influence a parameter of the motor (10; 10').
6. The arrangement as defined in one or more of the foregoing claims,
in which there is provided, parallel to one branch (22) of the first
voltage divider (20, 22), a second voltage divider (160) having a
tapping point (163), the potential at the latter tapping point (163)
influencing a parameter of the motor (10; 10').
7. The arrangement as defined in claim 6, in which the second voltage
divider (160) has a higher resistance as compared to the branch (22) of
the first voltage divider (20, 22) to which it is connected in parallel.

8. The arrangement as defined in claim 6 or 7, in which the voltage division ratio of the second voltage divider (60) is designed so that when the potential at its tapping point (163) is used as a comparison potential, the result is a lower value for that comparison potential.

9. The arrangement as defined in one of more of the foregoing claims, in which the potential at the tapping point (18; 163) of the first and/or second voltage divider (20, 22; 160) defines a current limiting value (I_{ref}) for limiting the motor current (i).

10. The arrangement as defined in claim 9, having a nonvolatile memory element (14) which stores at least one time value (T_D) after whose expiration a switchover of said output (A) of the microprocessor (12) is accomplished in program-controlled fashion.

11. A method for controlling the startup of an electric motor with which a microcontroller or microprocessor, hereinafter called a microprocessor, is associated for control purposes, having the following steps:

after the motor is switched on, an acceleration time (T_s) is monitored;

during that acceleration time (T_s), the current limiting value (I_{ref}) of an arrangement for limiting the motor current (i) is set in program-controlled fashion to a first value ($I_{ref} = 1$);

when it is ascertained that the acceleration time (T_s) has expired, the current limiting value (I_{ref}) is switched over in program-controlled fashion to a second value ($I_{ref} = TST$) that is different from the first value.

12. The method as defined in claim 11, in which the second current limiting value is less than the first.

13. The method as defined in claim 11 or 12, in which, after the acceleration time (T_s) has expired, a determination is made as to whether motor current limiting is effective during a time span that exceeds a predefined time span;

and if such is the case, the current limiting value (I_{ref}) is switched over in program-controlled fashion to a third value ($I_{ref} = 0$).

14. The method as defined in one or more of claims 11 through 13, in which at least the acceleration time (T_s) is stored in a nonvolatile memory element (14) whose values can be entered and/or modified via a data bus (13, 15).

15. An arrangement for carrying out the method as defined in one or more of claims 11 through 14, in which the microprocessor (12) for program-controlled switchover of the current limiting value (I_{ref}) has at least one output (A) that can be switched over at least between a high and a low signal level and thereby influences the current limiting value (I_{ref}); and that signal level can be modified in program-controlled fashion during acceleration of the motor (10; 10').

16. The arrangement as defined in claim 15, in which the at least one output (A) can be switched over to a high-resistance state called the tristate state.

17. The arrangement as defined in claim 15 or 16, in which the output (A) serving to switch over the current limiting value is connected via a resistor (17) to the tapping point (18) of a first voltage divider (20, 22), the potential at that tapping point (18) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows, and the motor current (i) being interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

18. The arrangement as defined in claim 17, in which there is provided parallel to one branch (22) of the first voltage divider (20, 22) a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows, and the motor current (i) being interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

19. The arrangement as defined in claim 18, in which the second voltage divider (160) has a higher resistance as compared to the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

20. The arrangement as defined in claim 18 or 19, in which the voltage division ratio of the second voltage divider (60) is designed so that when the potential at its tapping point (163) is used as a comparison potential, the result is a lower value for that comparison potential.

21. The arrangement as defined in one or more of claims 17 through 20, in which the voltage (u) at the measurement resistor (36) is filtered through a low-pass element (38, 42) before comparison with the aforesaid potential.

22. The arrangement as defined in claim 21, in which the low-pass element is configured as a first-order low-pass element (38, 42).

23. An arrangement having an electric motor (10; 10'), in particular for driving a fan (73),

having a microcontroller (12) or microprocessor, hereinafter simply called a microprocessor, for influencing at least one motor function,

having a nonvolatile memory element (14) for storing at least one variable as a definition for that motor function;

and having an interface (13a), associated with the electric motor, for a data line (13) for transferring that at least one variable to and/or from the nonvolatile memory element (14).

24. The arrangement as defined in claim 23, in which the microprocessor (12) is connected (lines 210, 226) to the interface (13a) for the data line (13);

and the transfer of data from and/or to the nonvolatile memory element (14) is accomplished via the microprocessor (12).

25. The arrangement as defined in claim 23 or 24, in which the data line is configured as a serial data bus (13, 210, 226).

26. The arrangement as defined in claim 25, in which there is associated with the microprocessor (12) a stored directory (280) which contains, for objects that are transferable via the data line (13, 210, 226), predefined parameters (286, 288, 290) for the transfer of those objects.

27. The arrangement as defined in claim 26, in which the stored directory (280) contains data (286) as to the length of transferable objects.
28. The arrangement as defined in claim 26 or 27, in which the stored directory (280) contains data (288) as to whether the relevant object is intended for storage in the nonvolatile memory element (14) or in a volatile memory element (330).
29. The arrangement as defined in one or more of claims 26 through 28, in which the stored directory (280) contains data (290) as to the address of the object in a memory element (14, 330).
30. The arrangement as defined in one or more of claims 23 through 29, in which the stored directory (280) is stored in nonvolatile and, in particular, permanent fashion in a memory (336) associated with the microprocessor (12).
31. The arrangement as defined in claim 30, in which the stored directory (280) is a hardware component of the microprocessor (12).
32. The arrangement as defined in one or more of claims 23 through 31, in which at least one buffer memory (332) for data traffic with a data line (13; 15) is provided in a volatile memory (330) associated with the microprocessor (12).
33. The arrangement as defined in one or more of claims 23 through 32, in which the nonvolatile memory element (14) is connected via a serial bus (15) to the microprocessor (12).
34. The arrangement as defined in claim 33, in which the nonvolatile memory element (14) is connected via a line (CS) to the microprocessor (12) which, controlled by the microprocessor (12), influences a write protection of the nonvolatile memory element (14).
35. The arrangement as defined in one or more of claims 23 through 34, in which the microprocessor (12) has a predefined memory element (332) for storing an address (FIG. 17: 242; FIG. 18: 254) conveyed via the data line (13), an arrangement (14, 330) for storing an address (324) of the arrangement to be addressed, and a comparison arrangement for comparing those two addresses.

36. The arrangement as defined in one or more of claims 23 through 35, in which a memory element (332) for storing a variable (FIGS. 18, 19: 246; FIG. 18: 254) that characterizes an object to be transferred is associated with the microprocessor (12); and by way of that variable, at least one characteristic (286, 288, 290) of that object can be taken, for processing thereof, from a directory (280) stored in the arrangement.

37. The arrangement as defined in claim 36, in which the characteristic is the length (286) of that object.

38. The arrangement as defined in claim 36 or 37, in which the characteristic is the hardware address (288, 290) of that object.

39. Use of an arrangement and/or a method as defined in one or more of the foregoing claims in a motor (10; 10') that drives a fan (73; 340).

40. The use as defined in claim 39, in which the fan is an equipment fan (340A, 340B, 240C).

U.S. Pat. No. 5,442,441

[amended Claims]

PCT/EP99/03992
July 13, 2000
P61.12PCT215
PCT-3037

Claims

1. An arrangement having an electric motor (10; 10'),
having a microcontroller (12) or microprocessor, hereinafter
simply called a microprocessor, for influencing at least one motor
function,
in which arrangement an output (A) of the microprocessor (12) can
be switched over in program-controlled fashion to a high level or to a
low level;
and a tapping point (19) [sic] of a first voltage divider (20, 22)
is connected to that terminal via a resistor (17) in order to make the
potential of that voltage divider tapping point (18) switchable in
program-controlled fashion between at least two values by modifying that
level, and by way of that potential to influence a parameter of the
motor (10; 10').
2. The arrangement as defined in claim 1, in which the parameter is a
current limiting value (I_{ref}) for limiting the motor current (i) of the
electric motor (10; 10').
3. The arrangement as defined in claim 1 or 2, in which said resistor
(17) is of high-resistance configuration.
4. The arrangement as defined in claim 3, in which the value of said
resistor (17) is 50 kilohm or more.
5. The arrangement as defined in one or more of claims 1 through 4,
in which said output (A) of the microprocessor (12) can be switched over
in program-controlled fashion to a third, high-resistance state (FIG.
4).

controlled fashion to a second value ($I_{ref} = TST$) that is different from the first value.

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12. The method as defined in claim 11, in which the second current limiting value is less than the first.

13. The method as defined in claim 11 or 12, in which, after the acceleration time (TS) has expired, a determination is made as to whether motor current limiting is effective during a time span that exceeds a predefined time span;

and if such is the case, the current limiting value (Iref) is switched over in program-controlled fashion to a third value (Iref = 0).

14. An arrangement for carrying out the method as defined in one or more of claims 11 through 13, in which the microprocessor (12) for program-controlled switchover of the current limiting value (Iref) has at least one output (A) that can be switched over at least between a high and a low signal level and thereby influences the current limiting value (Iref);

and that signal level can be modified in program-controlled fashion during acceleration of the motor (10; 10').

15. The arrangement as defined in claim 14, in which the at least one output (A) can be switched over to a high-resistance state called the tristate state.

16. The arrangement as defined in claim 14 or 15, in which the output (A) serving to switch over the current limiting value is connected via a resistor (17) to the tapping point (18) of a first voltage divider (20, 22), the potential at that tapping point (18) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows;

and the motor current (i) being interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

17. The arrangement as defined in claim 16, in which there is provided parallel to one branch (22) of the first voltage divider (20, 22) a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows;

and the motor current (i) being interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

18. The arrangement as defined in claim 17, in which a comparator (28) is provided for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows.

19. The arrangement as defined in claim 17 or 18, in which the second voltage divider (160) has a higher resistance as compared to the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

20. The arrangement as defined in one or more of claims 17 through 19, in which the voltage division ratio of the second voltage divider (60) is designed so that when the potential at its tapping point (163) is used as a comparison potential, the result is a lower value for that comparison potential.

21. The arrangement as defined in one or more of claims 16 through 20, in which the voltage (u) at the measurement resistor (36) is filtered through a low-pass element (38, 42) before comparison with the aforesaid comparison potential.

22. The arrangement as defined in claim 21, in which the low-pass element is configured as a first-order low-pass element (38, 42).

23. An arrangement having an electric motor (10; 10'), in particular for driving a fan (73),

having a microcontroller (12) or microprocessor, hereinafter simply called a microprocessor, for influencing at least one motor function, there being associated with that microprocessor (12) a volatile memory element (330) and a nonvolatile memory element (14), which memory elements being configured for storing at least one object as a definition for that motor function;

further having an interface (13a), associated with the electric motor, for a data line (13; 210, 226) for transferring that at least one object to and/or from a memory element (14, 330),

and having a stored directory (280), associated with the microprocessor (12), which contains, for objects that are transferable via the data line (13, 210, 226), predefined parameters (286, 288, 290) for the transfer of those objects.

24. The arrangement as defined in claim 23, in which the stored directory (280) contains data (286) as to the length of transferable objects.

25. The arrangement as defined in claim 23 or 24, in which the stored directory (280) contains data (288) as to whether the relevant object is intended for storage in the nonvolatile memory element (14) or in a volatile memory element (330).

26. The arrangement as defined in one or more of claims 23 through 25, in which the stored directory (280) contains data (290) as to the address of the object in a memory element (14, 330).

27. The arrangement as defined in one or more of claims 23 through 26, in which the stored directory (280) is stored in nonvolatile and, in particular, permanent fashion in a memory (336) associated with the microprocessor (12).

28. The arrangement as defined in claim 27, in which the stored directory (280) is a hardware component of the microprocessor (12).

29. The arrangement as defined in one or more of claims 23 through 28, in which the microprocessor (12) is connected to the interface (13a) for the data line (13);

and the transfer of objects from and/or to the nonvolatile memory element (14) is accomplished via the microprocessor (12).

30. The arrangement as defined in one or more of claims 23 through 29, in which the data line is configured as a serial data bus (13, 210, 226).

31. The arrangement as defined in one or more of claims 23 through 30, in which at least one buffer memory (332) for data traffic with a data line (13; 15) is provided in the volatile memory (330) associated with the microprocessor (12).

32. The arrangement as defined in one or more of claims 23 through 31, in which the nonvolatile memory element (14) is connected via a line (CS) to the microprocessor (12) which, controlled by the microprocessor (12), influences a write protection of the nonvolatile memory element (14).

33. The arrangement as defined in one or more of claims 23 through 32, in which the microprocessor (12) has a predefined memory element (332) for storing an address (FIG. 17: 242; FIG. 18: 254) conveyed via the data line (13), an arrangement (14, 330) for storing an address (324) of the arrangement to be addressed, and a comparison arrangement for comparing those two addresses.

34. The arrangement as defined in one or more of claims 23 through 33, in which a memory element (332) for storing a variable (FIGS. 18, 19: 246; FIG. 18: 254) that characterizes an object to be transferred is associated with the microprocessor (12);

and by way of that variable, at least one characteristic (286, 288, 290) of that object can be taken, for processing thereof, from a directory (280) stored in the arrangement.

35. The arrangement as defined in claim 34, in which the characteristic is the length (286) of that object.

36. The arrangement as defined in claim 34 or 35, in which the characteristic is the hardware address (288, 290) of that object.

37. Use of an arrangement and/or a method as defined in one or more of the foregoing claims in a motor (10; 10') that drives a fan (73; 340).

38. The use as defined in claim 37, in which the fan is an equipment fan (340A, 340B, 240C).

Abstract

1 An arrangement having an electric motor (10) has a
2 microcontroller (12) for influencing at least one motor
3 function and a nonvolatile storage element (14) for storing
4 at least one variable as a definition for that motor
5 function. The arrangement also has an interface (13a) for a
6 data line (13) for transferring the at least one variable,
7 in particular a current limiting value (I_{ref}) from or to a
8 storage element (14) by way of the microcontroller (12), and
9 optionally by way of an internal data bus (15). The
10 invention also relates to use of the device in the context
11 of batteries of fans, and program-controlled current
12 limitation for startup of an electric motor (10).

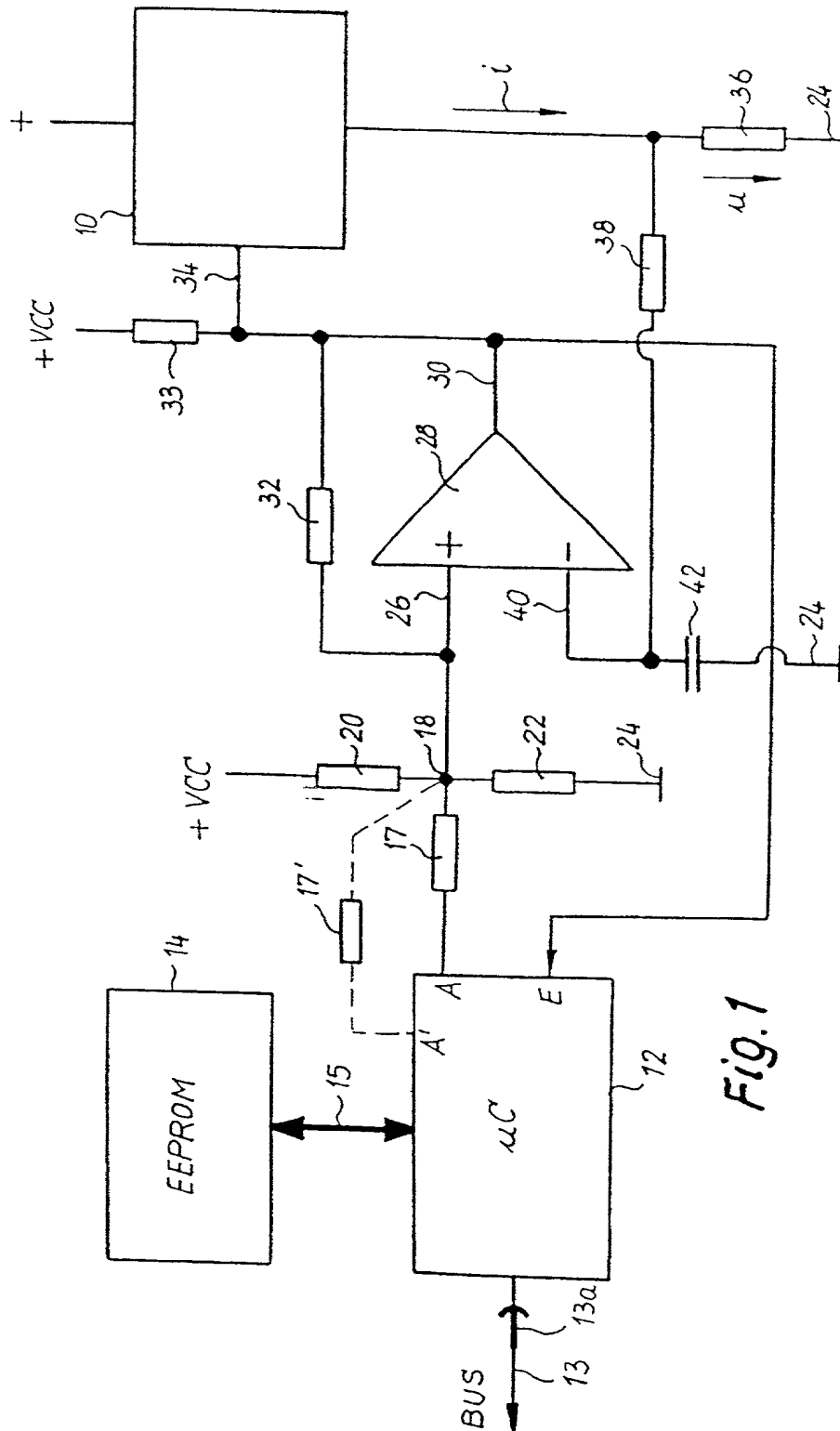


Fig. 1

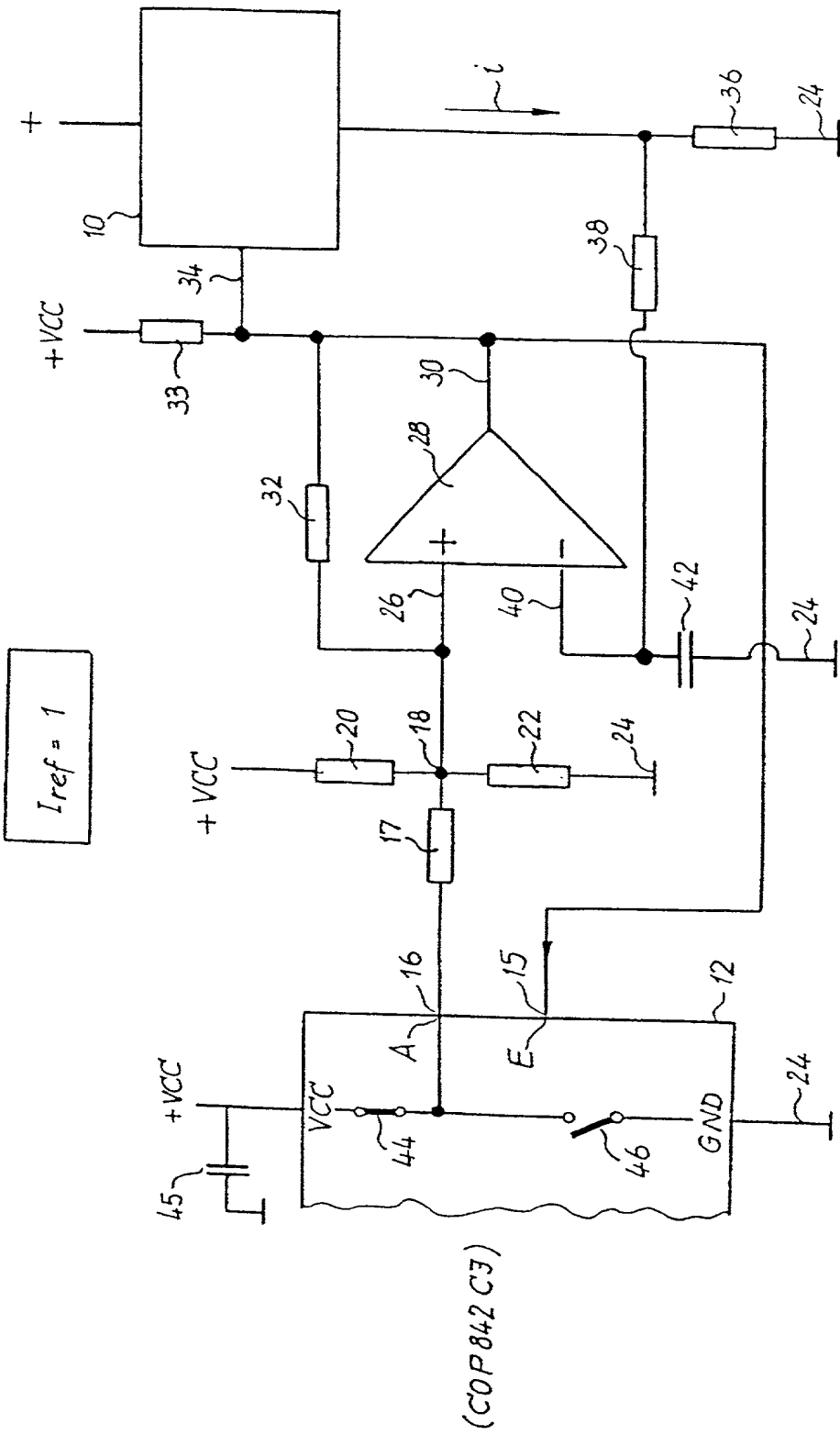


Fig. 2

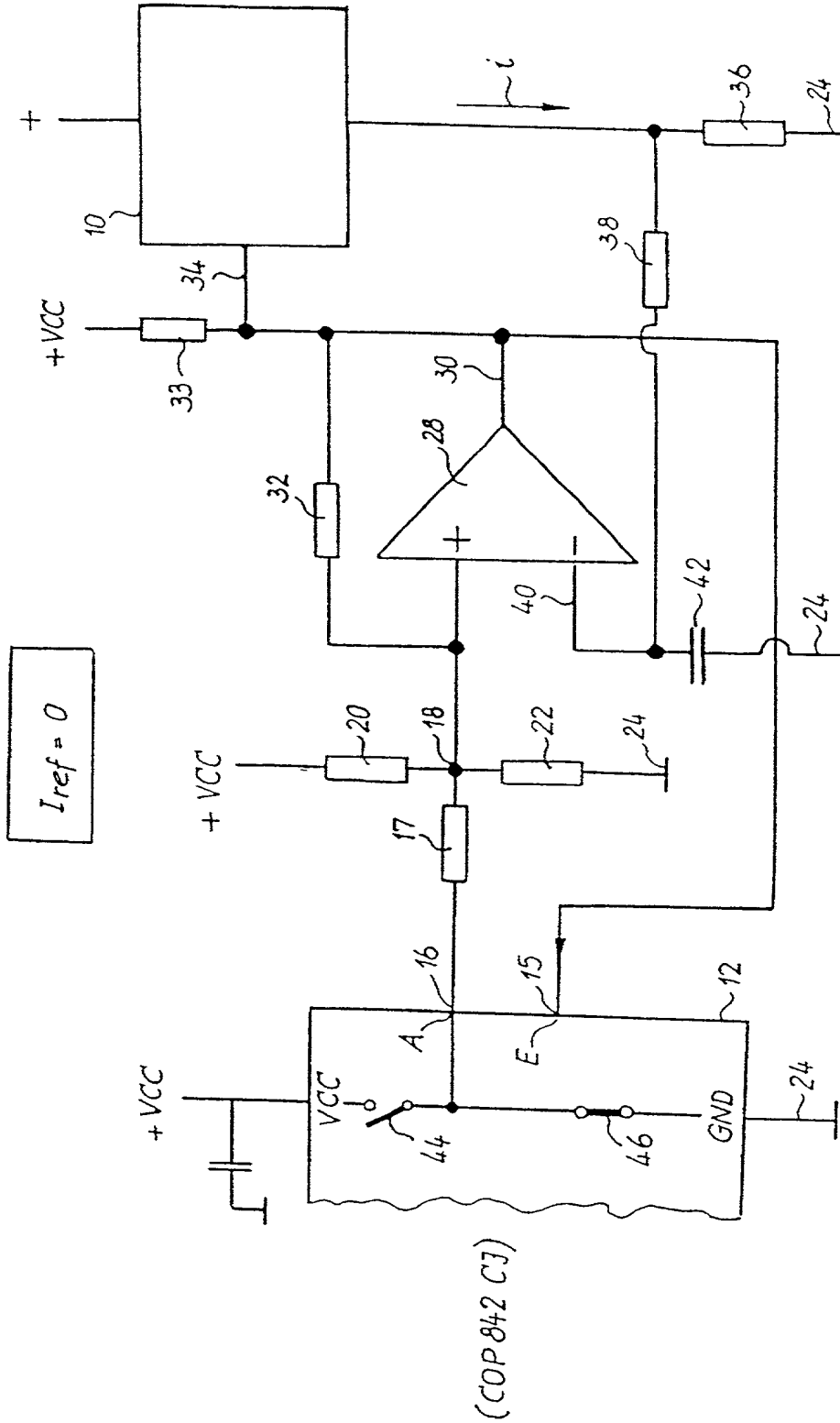


Fig. 3

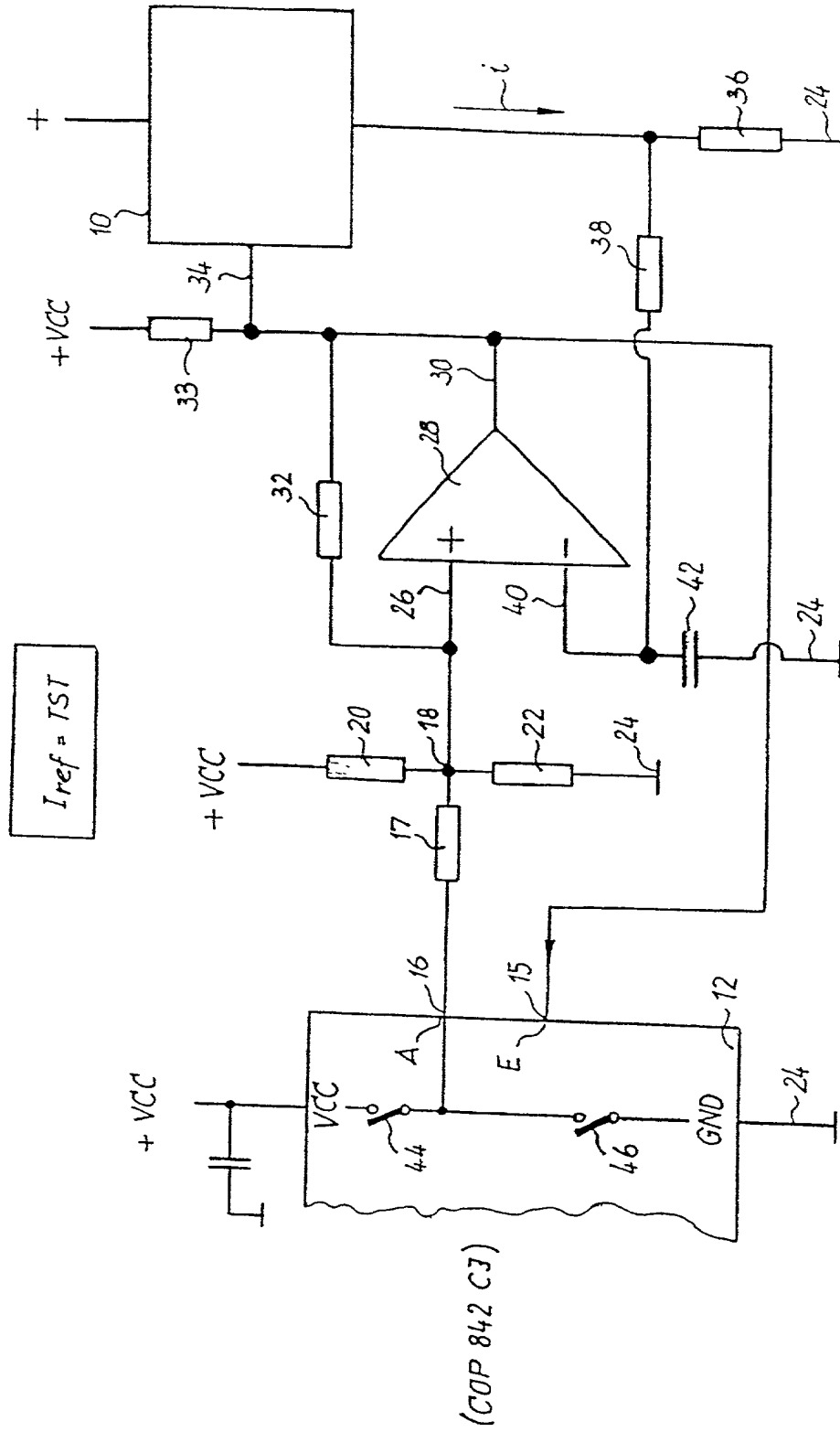


Fig. 4

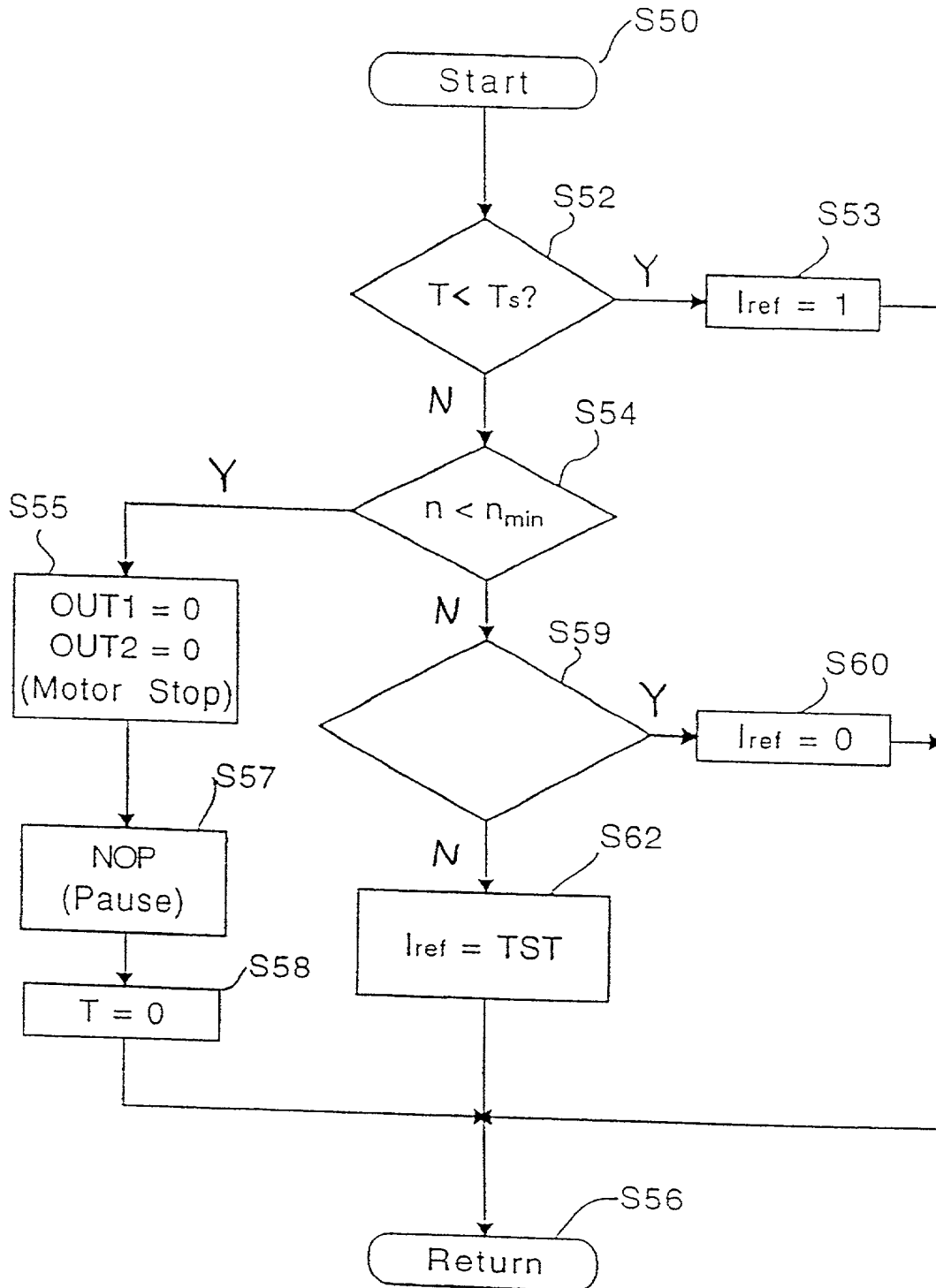


Fig. 5

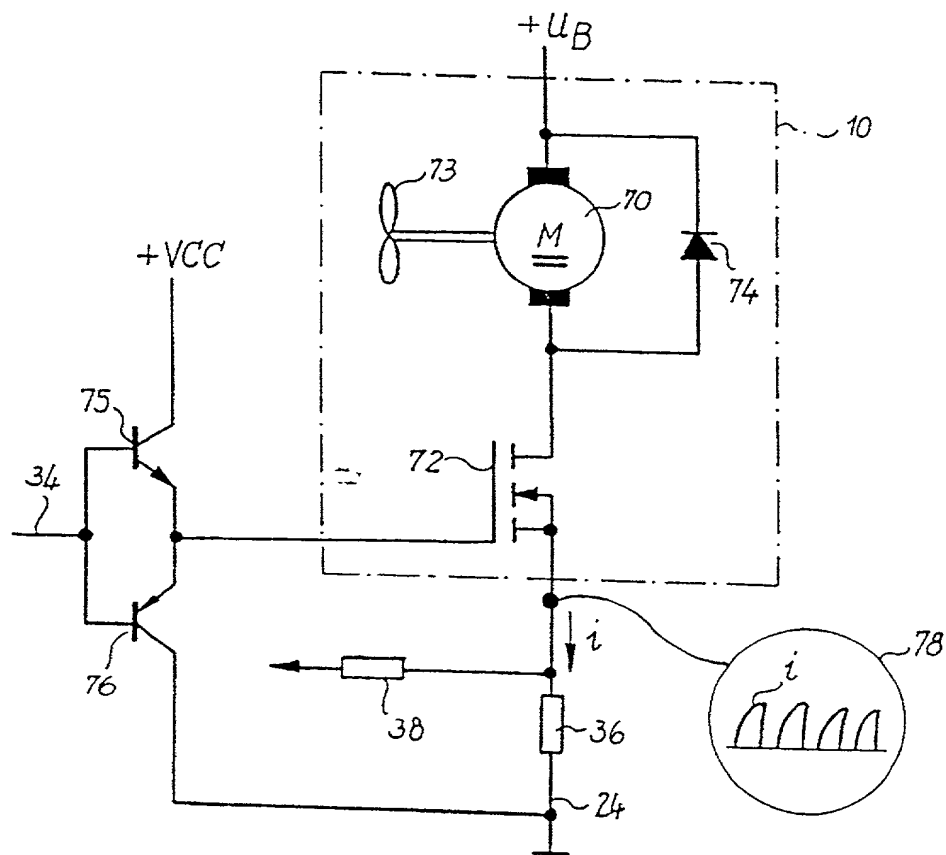


Fig. 6

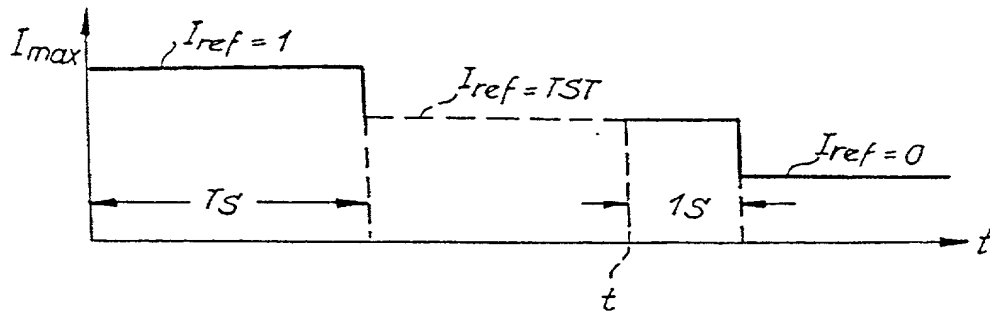


Fig. 7

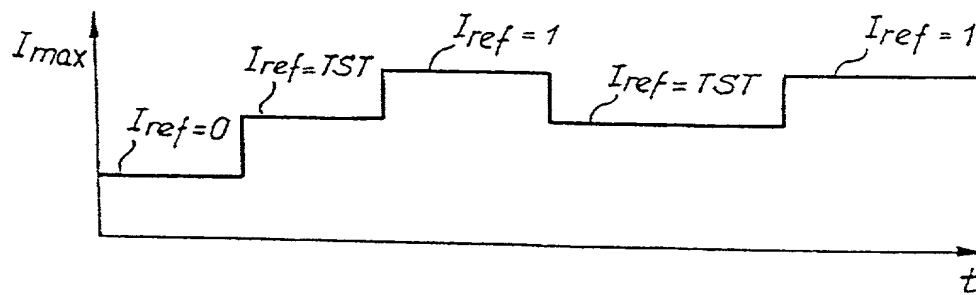


Fig. 8

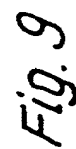


Fig. 9

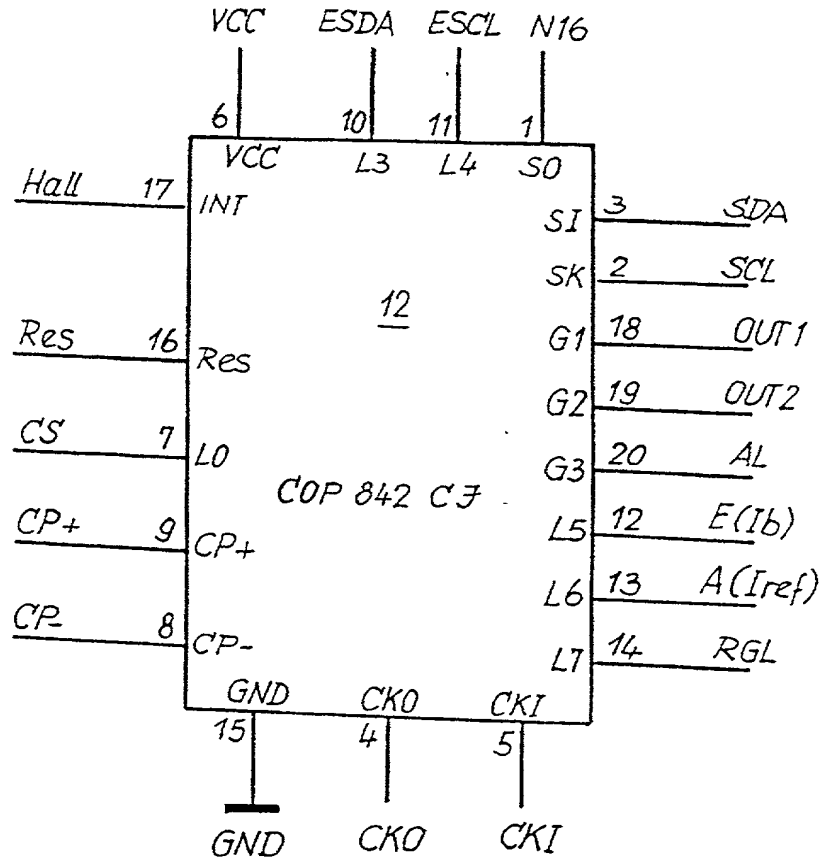


Fig. 10

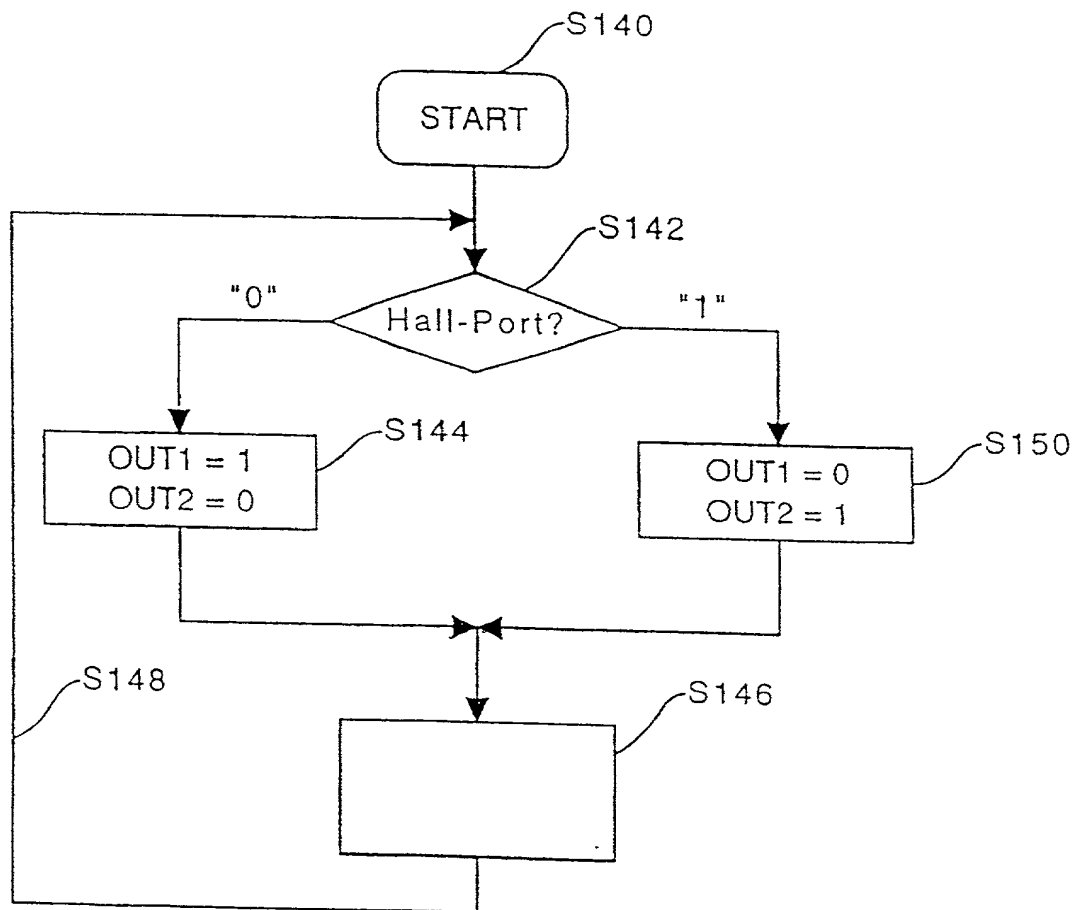
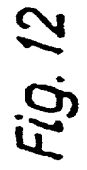


Fig. 11



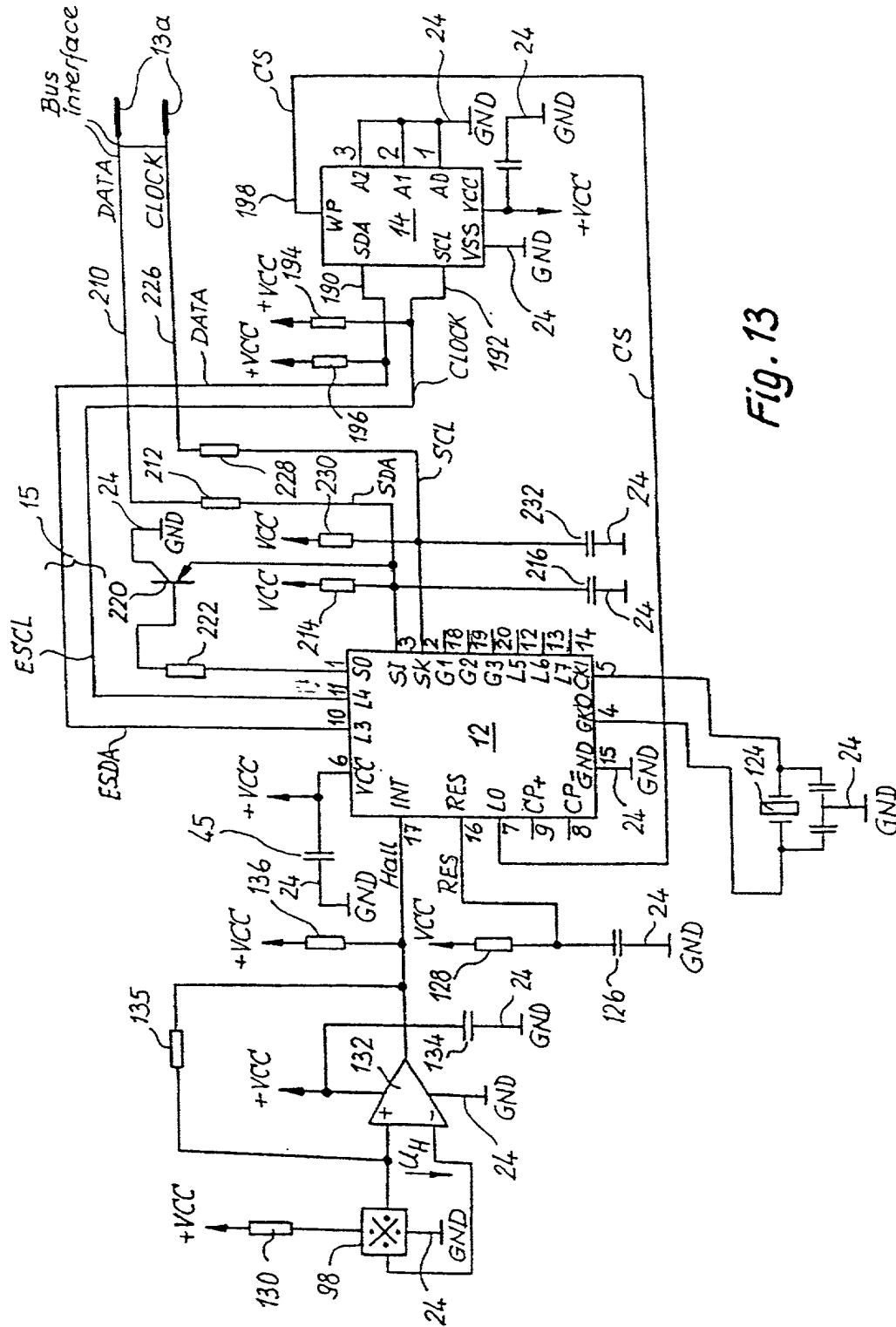


Fig. 13

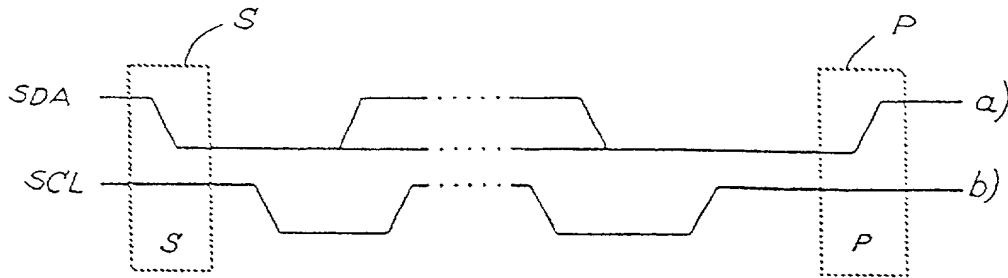


Fig. 14

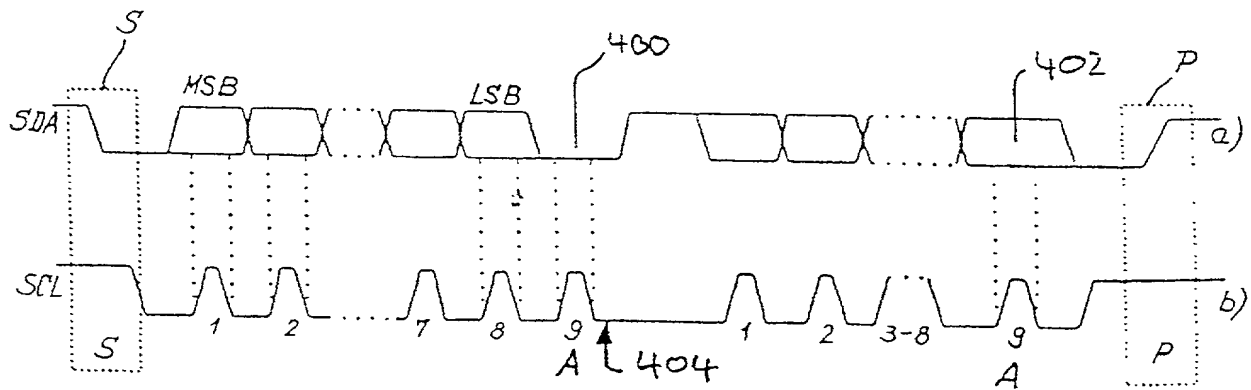


Fig. 15

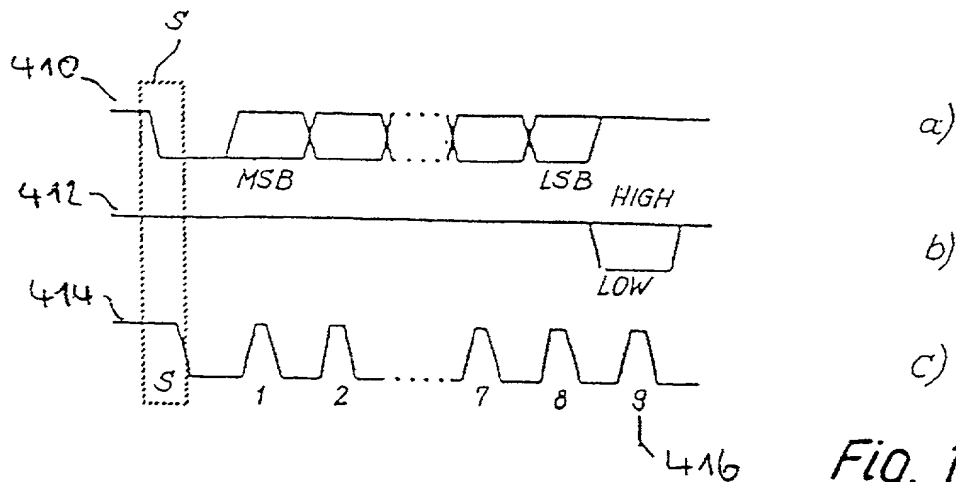


Fig. 16

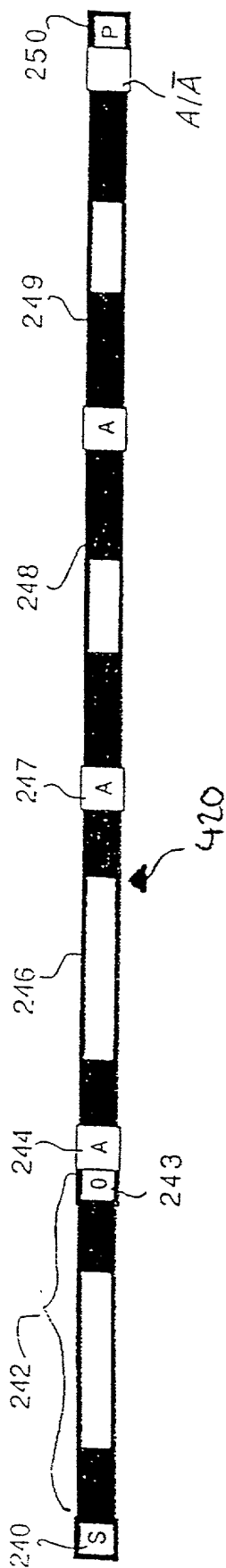


Fig. 17

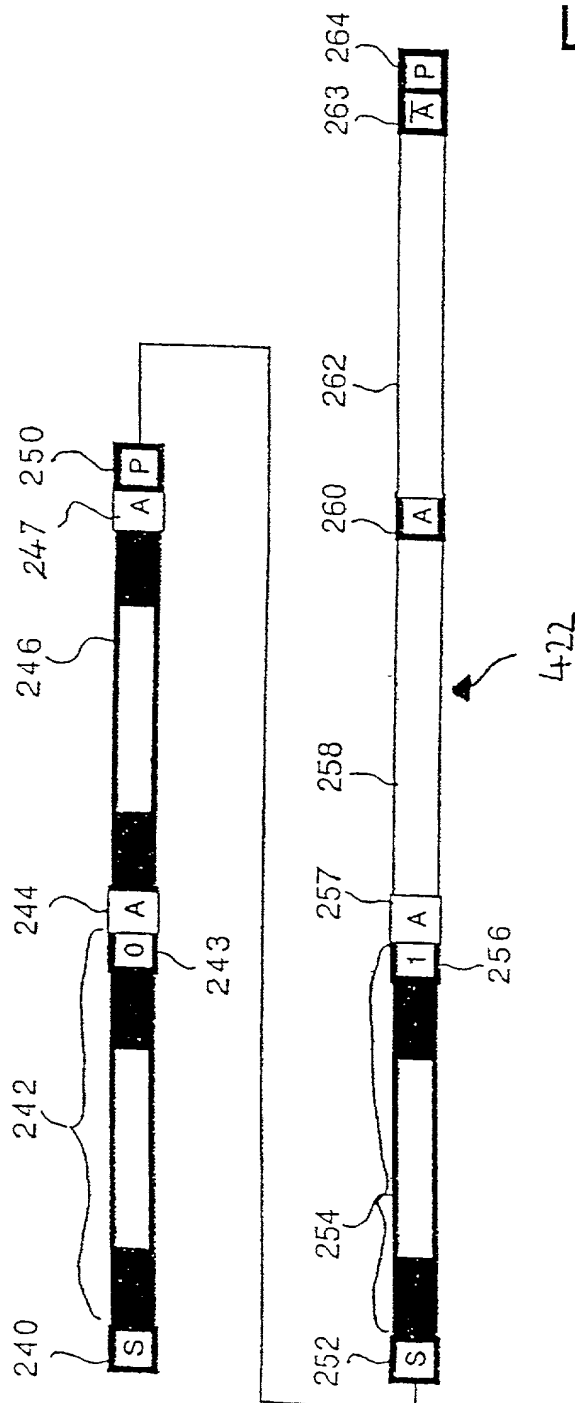


Fig. 18

280		282		284		286		288		290	
AA		BB		CC		DD		EE			
01		B1		1		EEPROM		0x00			
02		B2		1		RAM		0x00			
03		B3		2		EEPROM		0x01			
04		B4		2		RAM		0x01			
...				
...				
32		B32		1		ROM		0x00			
33		B33		1		ROM		0x01			
...				

Fig. 19

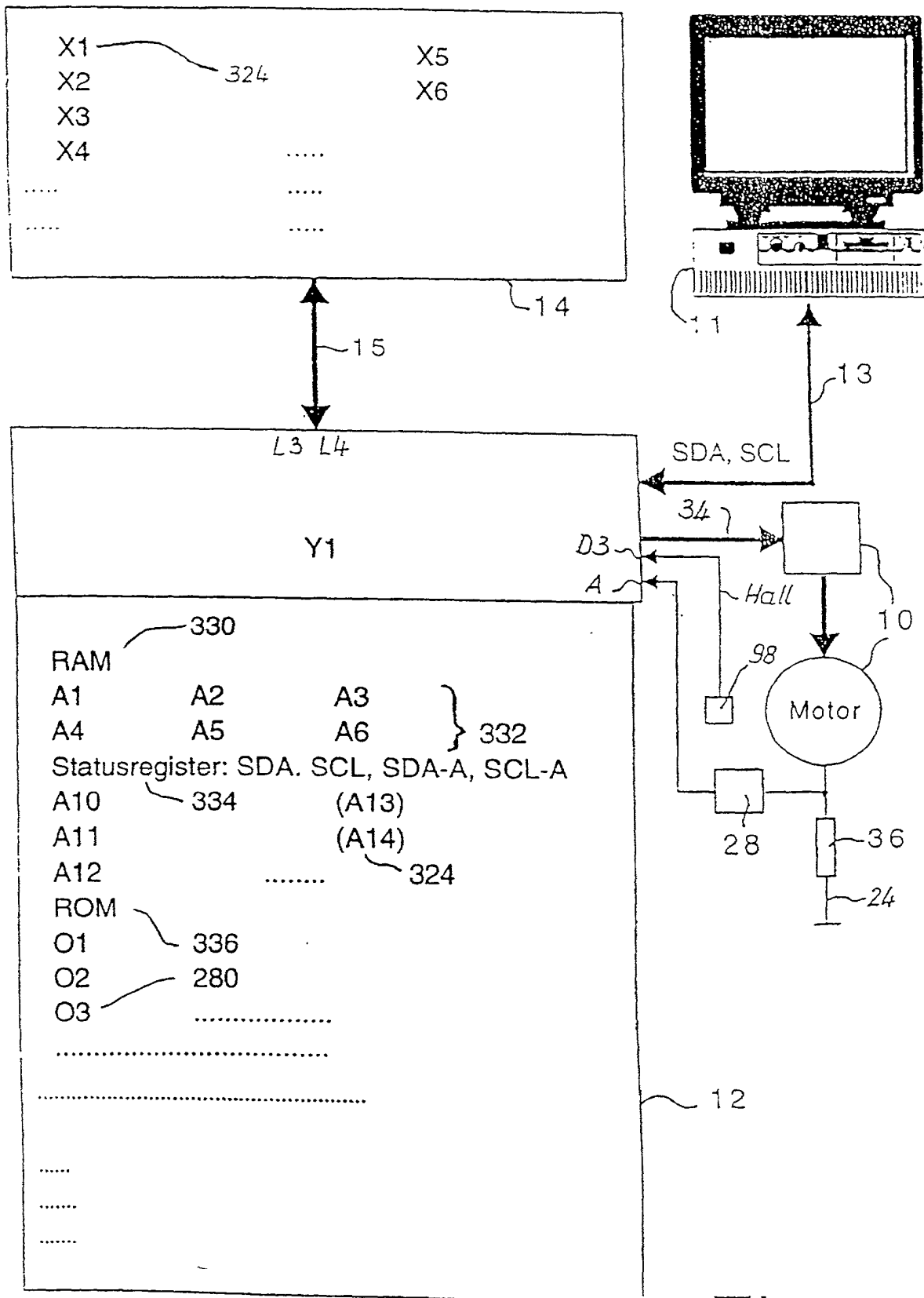


Fig. 20

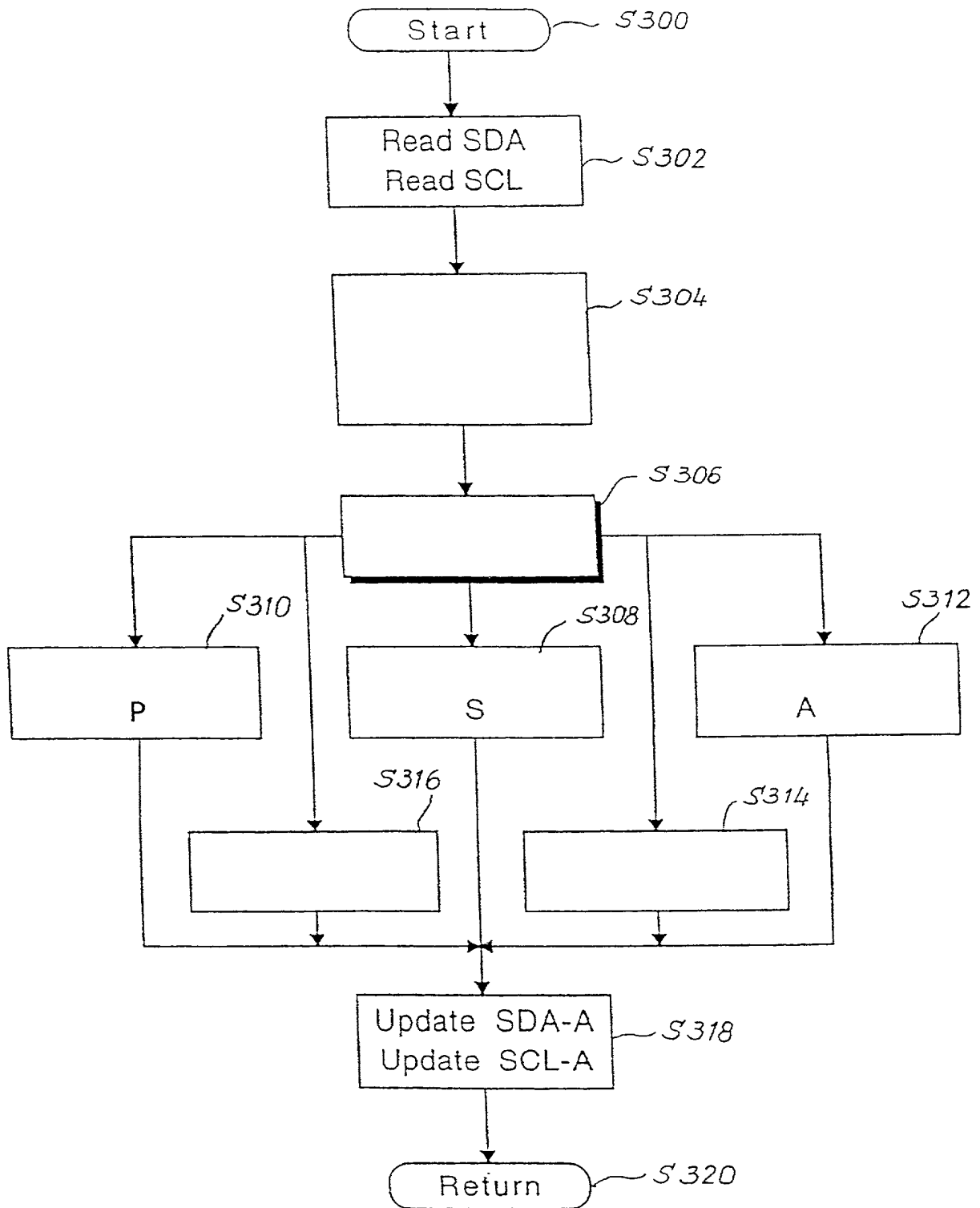


Fig. 21

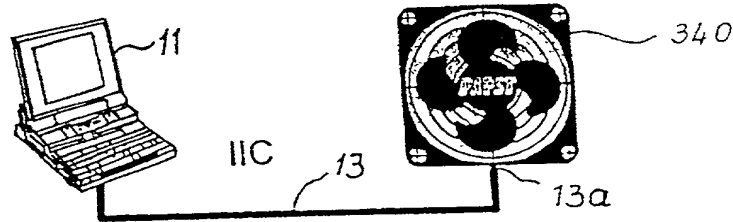


Fig. 22

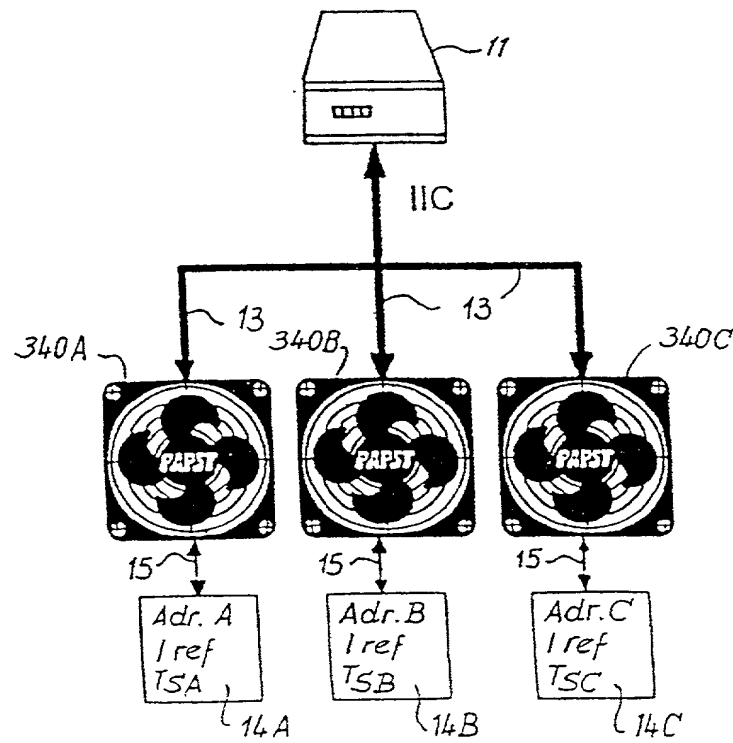


Fig. 23

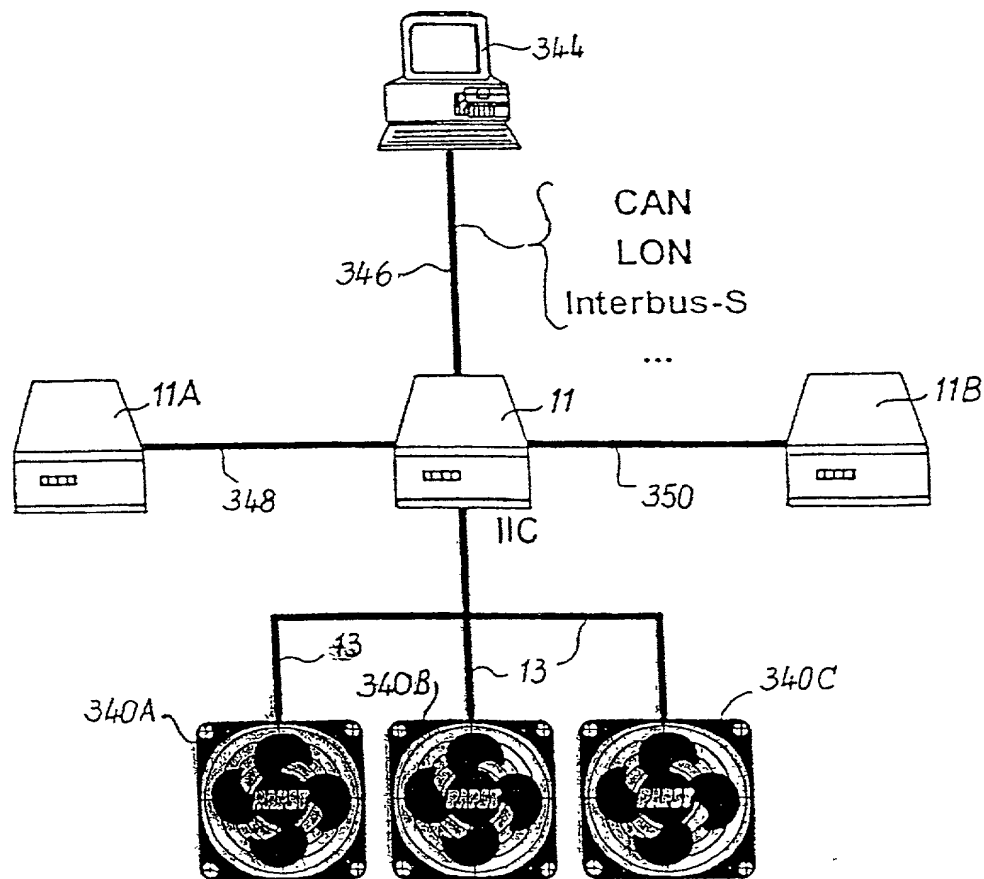


Fig. 24

DECLARATION & POWER OF ATTORNEY FOR PATENT APPLICATION
ERKLÄRUNG FÜR PATENTANMELDUNG, MIT VOLLMACHT

GERMAN-LANGUAGE DECLARATION

Als nachstehend benannter Erfinder, erkläre ich hiermit an Eides Statt:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen;

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

Anordnung mit einem Elektromotor

deren Beschreibung
(zutreffendes ankreuzen)

☐ hier beigelegt ist.

☒ am 10. JUN. 1999 unter der internationale Anwendungsnummer PCT/EP99/03992 eingereicht wurde und am _____ abgeändert wurde (falls tatsächlich abgeändert).

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung, einschliesslich der Ansprüche, durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung, in Einklang mit Absatz 37, Bundesvorschriften, § 1.56(a) von Wichtigkeit sind, an.

Ich beanspruche hiermit ausländische Prioritätsvorteile, gemäss Abschnitt 35 der Bundesgesetze der Vereinigten Staaten, § 119, aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfinderurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfinderurkunde nachstehend gekennzeichnet, die ein Anmeldungsdatum haben, dass vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

As a below-named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject-matter which is claimed and for which a patent is sought on the invention entitled:

Device with an Electromotor

the specification of which
(check one)

☐ is attached hereto

☒ was filed on 10 JUN. 1999 as International Application Number PCT/EP99/03992 and was amended on _____ (if in fact amended).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119, of any foreign application(s) for patent or inventor's certificate listed below, and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

[illegible]

Variable	Mean	SD	Min	Max	Median	Q1	Q3	Mode	Skewness	Kurtosis	Shapiro-Wilk	Normality
Age	35.2	12.5	18	65	32	28	38	35	0.15	2.1	0.98	Normal
Gender	1.2	0.4	1	2	1	1	1	1	0.05	0.2	0.95	Normal
Education	12.5	2.1	9	16	12	11	13	12	0.12	1.8	0.97	Normal
Income	1500	500	500	3000	1200	800	1800	1000	0.25	3.5	0.92	Normal
Marital Status	1.5	0.5	1	2	1	1	1	1	0.08	0.3	0.96	Normal
Occupation	2.5	1.2	1	4	2	1	3	2	0.18	2.5	0.94	Normal
Health Status	1.8	0.6	1	2	1	1	1	1	0.02	0.1	0.99	Normal
Stress Level	3.2	1.5	1	5	3	2	4	3	0.22	3.2	0.91	Normal
Life Satisfaction	4.5	1.2	3	6	4	4	5	4	0.10	2.0	0.97	Normal
Work-Life Balance	3.8	1.0	2	5	3	3	4	3	0.14	2.3	0.96	Normal
Family Support	4.2	1.1	3	5	4	4	5	4	0.09	1.9	0.98	Normal
Community Involvement	2.8	1.3	1	5	2	1	3	2	0.20	3.0	0.93	Normal
Personal Growth	3.5	1.4	2	5	3	2	4	3	0.16	2.6	0.95	Normal
Overall Well-being	4.0	1.1	3	5	4	4	5	4	0.07	1.8	0.99	Normal

DECLARATION & POWER OF ATTORNEY FOR PATENT APPLICATION
ERKLÄRUNG FÜR PATENTANMELDUNG, MIT VOLLMACHT

GERMAN-LANGUAGE DECLARATION

10
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